VCO Design

***Abstract* – This assignment paper presents a class-b LC oscillator based VCO for use in a 2.45GHz transceiver for ISM band applications. The VCO is designed in a 65nm CMOS technology with all components integrated on-chip and consumes 812.2µW while operating from a 1V supply.**

Index Terms – Class-B, LC Oscillator, VCO, Phase Noise

I. Introduction

The performance requirements for the VCO are as follows:

LO Frequency (GHz)	Tuning Range (+/-)	Phase Noise Δf=100KHz (dBc/Hz)	Phase Noise Δf=10MHz (dBc/Hz)	FoM Δf=1MHz (dBc/Hz)
2.45	10%	-97	-130	186

The following sections will be covered in this paper: (II) Class-B LC oscillator design procedure (III) Tuning range approach (IV) Simulation results.

II. Class-B LC Oscillator Design Procedure

The design of a class-B LC oscillator much like other resonant systems starts with the design of the tank, primarily driven by the performance of the inductor available on-chip, in our case, the design process was as follows:

1. Choose the on-chip inductor with the largest LxQ product

The choice for the inductor will determine the tank equivalent resistance, and in turn the bias current (power consumption) needed to increase voltage swing to meet the phase noise specs. *Make sure to keep the self-resonant frequency (SRF) larger than your desired oscillating frequency (the SRF is largely determined by the parasitic capacitance of the inductor)*

we chose an inductor: $L=15.035\,nH \quad Q=15.992 \quad SRF=4.103\,GHz$

2. Estimate the necessary tank capacitance for oscillation at Fo

From $W_{osc}=\frac{1}{\sqrt{(L\,x\,C)}}$ we estimate $C_{tank}=\frac{1}{L\,x\,W_{osc}^2}=280.7\,fF$

This value will differ slightly due to other parasitic capacitances found across the tank nodes (in the order of tens of fF maximum).

3. Estimate the equivalent Tank Resistance Rp

This is the parasitic resistance due non-ideal Q of on-chip inductor. $R_p=W_{osc}\,x\,L_{tank}\,x\,Q_l=3.701\,k\Omega$ *Q of capacitor is also important when capacitors are poor (as we'll see in tunability section) and at higher frequencies.*

4. Estimate bias current for Maximum Oscillation Amplitude

Recall to minimize phase noise we should bias the LC Oscillator to attain the largest differential voltage swing at the output: By increasing the current until the voltage swing no longer increases (i.e. the oscillator is operating in the voltage limited regime).

Normally for a class-B VCO the voltage limited regime is reached at an ideal $V_{osc\_diff\_peak}=2\,xVdd$ or 2V in our case. *Note choosing a bias point around 0.8 to 0.9 of max amplitude may be more adequate (decreasing returns to scaling current at the high end), and additionally we must be mindful not to exceed the maximum voltage rating across the drain to gate node for the particular transistor in the technology.* For 1V devices we are limited to 1.2V maximum, hence we opted to use thick-oxide 2.5V devices for the cross-coupled pair. Given our $V_{osc\_diff\_peak}=R_p\,x\,I_{peak\_wo}$, where Ipeak is our peak current at resonance: $I_{peak\_wo}=I_{bias}\,x\,\alpha$ and the α factor is inversely proportional to the conduction angle given by the topology ($\alpha=2/\pi$ for a Class-B LC oscillator). We can estimate $I_{bias}=\frac{V_{osc\_diff\_peak}}{R_p\,x\,\alpha}=\frac{V_{osc\_diff\_peak}}{R_p}\,x\,\frac{\pi}{2}=848.8\,\mu A$

5. Calculate minimum gm condition for oscillation start-up

In order to compensate for the losses of the tank in order to sustain oscillation, we require positive feedback with a minimum trans-conductance gain given by: $gm_{0,1}>2/R_p$ in our case $gm_{0,1}>540.4\,\mu S$ *Note gm must be considerably larger than minimum to guarantee oscillation and complete switching (current steering between M0 and M1), additionally it is recommended to employ fingers for width and minimum length devices to minimize parasitic capacitances which could affect LC tank performance.*

At this point, we went to our device characterization testbench and biased our test transistor at our desired constant-current (Ibias/2) then we swept the device's width and found the optimal width where gm/Id is largest. In our case then: $W_{0,1}=5.2\,\mu m$ and $L_{0,1}=L_{min}=280\,nm$ for thick-oxide 2.5V devices.

6. Sizing of the tail current source

The size of the tail current mirror device was a very important design choice: it can introduce flicker noise which is then up-converted by the oscillator to our target frequency (becoming $1/f^3$ noise) degrading our performance. Hence, it was one of our design "knobs", whereby increasing it's width allowed for both increases in current (and hence swing amplitude), and a reduction in flicker noise: contributing to reductions in phase noise at the cost of current consumption. For our initial design estimate $W_2=40\,\mu m$ with $L_2=L_{min}=60\,nm$ for standard 1V devices.

III. Tuning Range Approach

With our designed class-B LC oscillator above, we now explored two strategies to achieve a frequency tuning range of +/-10%.

Continuous tuning

Initially, we explored the use of continuous tuning only (with the use of NMOSCAP varactors available in the TSMC65nm technology), the following was our initial general procedure:

1. Set min. tank capacitance to yield Fosc+10% (2.695GHz)

2. Choose varactor size to cover frequency range down to Fosc-10% (2.205GHz) given an available control voltage of 1V.

3. Choose varactor orientation to lead to effective vgate of -1 to 0V range. (capacitance is more linear in weak accumulation and depletion region)

4. Iterate choice of fixed tank capacitor, given minimum varactor capacitance to meet max frequency.

5. Iterate choice of varactor size as needed to cover min frequency.

6. Sweep frequency to locate Vcontrol needed for 2.45GHz.

7. Assess phase noise performance over tuning range.

With a single varactor and the continuous tuning strategy above, it was possible to meet the tuning range and phase noise specifications at our target frequency (phase noise at 100KHz offset was the most stringent spec to meet), however the large varactor needed to cover frequency range, degraded substantially the Q of the tank (introduces losses, especially so at large capacitance: minimum frequency end) and hence required us to increase the tail current mirror many-fold (~1.7mA Ibias) in order to increase amplitude swing to meet our phase noise specs, additionally it was very tedious to optimize component values to both cover the range while preserving our phase noise low. A more viable and practical approach was to use discrete tuning with a capacitor bank plus a limited range of continuous tuning provided with a smaller sized varactor.

Discrete tuning plus limited continuous tuning

In our case, a single capacitor bank (single-bit) was sufficient for our purposes. Enabling the cap bank (with varactor at minimum capacitance) allowed for one discrete step from our maximum frequency down to our target 2.45GHz frequency, here we can operate with lowest phase noise as the effects of our varactor are minimum. Additionally our varactor only needs to cover half the range from before (with some margin for overlap). *Note it is important to choose the size of the NMOS switches for the capacitor-bank appropriately as they will introduce losses degrading Q of the tank (and reducing amplitude swing) which will impact the phase noise adversely.* The general tuning range procedure in our case was as follows (similar from before):

1. Set fixed tank capacitance to yield Fosc+10% (2.695GHz)

2. Set cap-bank capacitance to switch freq. to 2.45GHz target when enabled

- Use ideal switches initially.

3. Choose varactor size in order to cover half range from before.

- From Fmax to Fosc, and then from Fosc to Fmin

4. Iterate on choice of tank cap. given minimum varactor freq.

5. Iterate on choice of cap bank size to switch to 2.45GHz when set

6. Assess phase noise performance over tuning range (with ideal switches)

7. Replace ideal switches with NMOS transistors

- Characterize degradation in performance

8. Keeping min. length, sweep width to find optimal device size.

- Find optimal point where decreasing ON switch resistance and increasing parasitic capacitances are traded-off optimally. (where phase noise response is smallest)

9. Assess phase noise performance over tuning range (all on-chip components)

10. Increase (tune) the size of tail current mirror modestly as needed to meet noise specs

- Increase bias current to increase oscillator voltage swing
- while decreasing flicker noise

IV. Simulation Results

Figure 1. Our final Class-B LC-based VCO **schematic with annotated component values** (all integrated components)

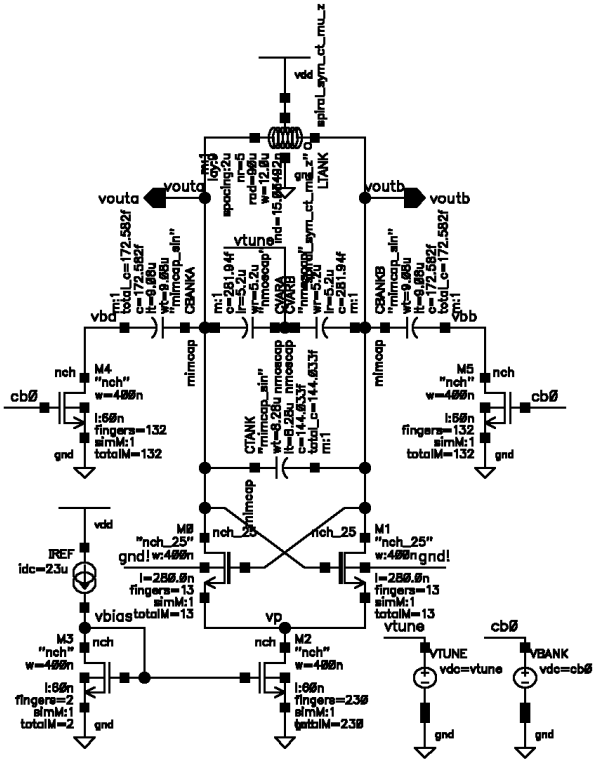


Figure 2. Transient voltage waveforms at both output nodes (2.45GHz). *Note period (center) and annotated minimum and maximum voltage differences below 2.5V for thick-oxide devices.*

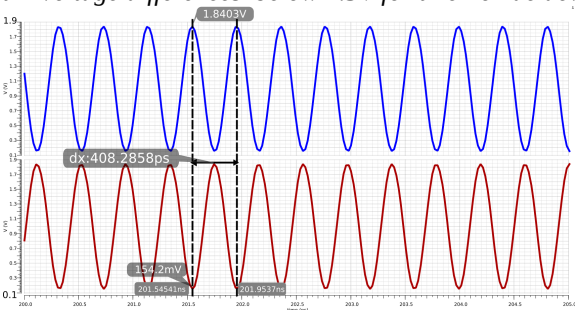


Figure 3. Frequency vs. Vcontrol with and without cap-bank enabled (over full frequency range)

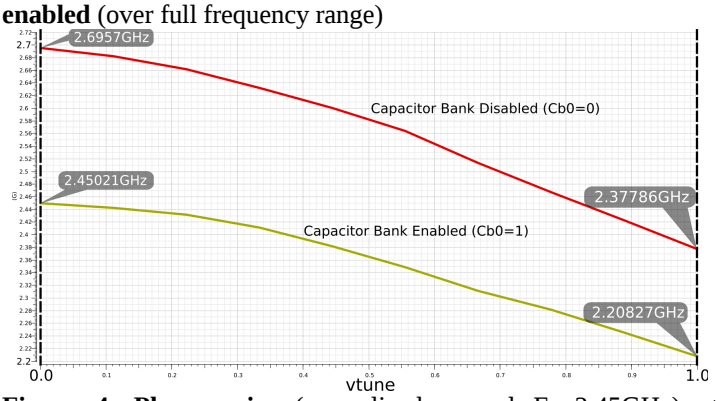
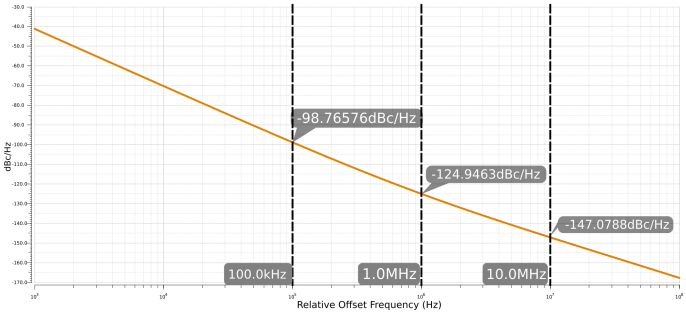


Figure 4. Phase noise (normalized around Fc=2.45GHz) at **100KHz, 1MHz and 10MHz offsets** (pss plus pnoise analyses)



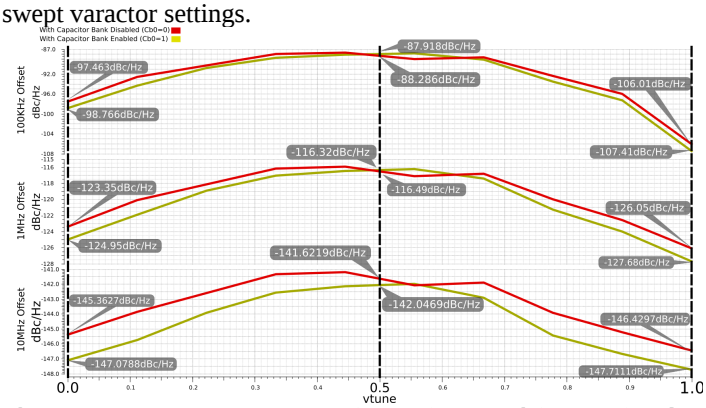
The Figure of Merit for our oscillator design (at 1 MHz Offset)

$$FoM_{osc} = 20\log\left(\frac{f_{osc}}{\Delta f}\right) - PN(\Delta f) - Power(dBm)$$ hence in our case:

$$FoM_{osc} = 20\log\left(\frac{2.45\,GHz}{1\,MHz}\right) - (-124.946\,dBc/Hz) - 10\log\left(\frac{812.2\,\mu W}{1\,mW}\right)$$

$$FoM_{osc} = 193.63\,dBc/Hz$$

Figure 5. An interesting plot to consider, is how our phase noise changes (at our defined offsets) at different capacitor bank and swept varactor settings.



Phase noise is minimum at our max (2.7GHz), nominal (2.45GHz) and min (2.2GHz) frequencies, but degrades in between these frequencies where the effective voltage across the varactor Vvar=-0.5V: Here the ΔC vs. ΔVvar slope is large, leading to greater phase noise due to large oscillating amplitude modulating Vvar and hence varactor capacitance.

References

[1] RF Microelectronics Textbook (Behzad Razavi): Oscillators Chapter

[2] Phase Noise in LC Oscillators: From Basic Concepts to Advanced Topologies (Carlo Samori): http://toronto.ieee.ca/files/2016/12/DL-VCO-short.pdf

[3] Fully Integrated Low Phase Noise LC VCO: http://pallen.ece.gatech.edu/Academic/ECE_6440/Summer_2003/L140-TonyVCO(2UP).pdf

[4] Analysis and Simulation of a CMOS VCO (Texas A&M University): http://ece.tamu.edu/~kentesar/ELEN665/lab5.pdf

[5] RF Harmonic Oscillators Integrated in Silicon Technologies: http://toronto.ieee.ca/files/2017/06/DL-Toronto.pdf

[6] The MOS Capacitor (University of Illinois): http://transport.ece.illinois.edu/ece340f11-lectures/ece340lecture39-mos_capii.pdf