Mixer Design

***Abstract* – This assignment paper presents a current-driven passive mixer down-converter and TIA for use in a 2.45GHz receiver for ISM band applications. The mixer and TIA are designed in a 65nm CMOS technology and consume 315.88µW.**

***Index Terms* – Low power, Passive Mixer, TIA, 2.45GHz, ISM**

I. Introduction

The performance requirements for the differential passive mixer down-converter and TIA are as follows:

LO Frequency (GHz)	Gain Differential (dB)	Output 3dB BW (MHz)	Linearity IP3 (dBm)	Input Referred Noise	TIA Power (mW)
2.45	30	2	10	$30\mu V_{rms}$	< 2

The following sections will be covered in this paper: (II) General Receiver Architecture (III) Receiver Simulation Test-bench (IV) Mixer Design procedure (V) TIA Design Procedure (VI) Results and discussion.

II. General Receiver Architecture

The RF receiver architecture is composed of: (1) an ideal low-noise transimpedance amplifier (LNTA) converts an input single-ended antenna voltage to a differential RF current. (2) A current-mode passive mixer then down-converts the RF current to a Zero or low IF baseband differential current and (3) a differential transimpedance amplifier converts the baseband current to a differential output voltage.

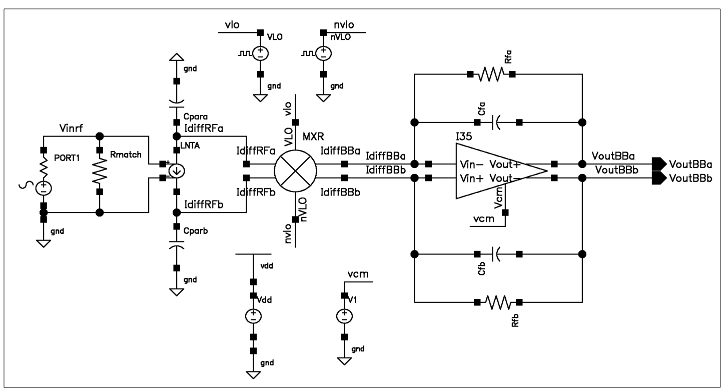

Figure 1: General Receiver Architecture

Note: we are modeling our ideal LNTA as a VCCS.

III. Receiver Simulation

We started the design process by modeling the receiver performance using an ideal differential Opamp (implemented with VCVS components); this allowed us to devise correct simulation analyses and parameters for each of the specifications to be met, hence decoupling the design of the Opamp from the receiver and mixer simulation.

Given a nominal input power of -50dBm (our starting test amplitude), the simplest and first analysis (albeit very limited) to verify quickly the functioning of the mixer is to apply a tone at RF plus a small offset frequency and inspect the down-converted low-IF transient waveform. Incrementally, we required the use of new advanced analysis to assess the performance of the mixer: periodic steady state analysis (PSS), periodic AC analysis (PAC), periodic noise analysis (PNOISE), quasi-periodic steady state analysis (QPSS) and quasi-periodic AC analysis (QPAC). We used these analyses [1], [2], [3] in order to calculate our required specs: Voltage conversion gain versus RF frequency, Output -3dB bandwidth, Input referred noise and Linearity.

IV. Passive Mixer Design Procedure

Passive mixers as their name implies make use of transistors operating largely between triode and cutoff (much like digital switches), this makes them very much amenable at small (and decreasing) modern technology nodes. The general topology of the current-mode differential passive mixer is the following:

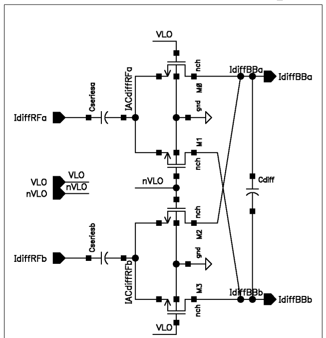

Figure 2: Passive MXR

For the passive mixer we started the design by understanding the minimum width of the device, governed primarily by the ON resistance of the switch and parasitic capacitance at the preceding node which forms a current filter and can limit our bandwidth and hence conversion gain of the mixer, mainly: $R_{on}=\frac{1}{2x\pi f_{lo}C_{par}}$

1. We would like to choose the size of the mixer switches to yield adequate bandwidth and support operation at our local oscillator frequency of 2.45GHz. Given our prior node parasitic capacitance of 100fF, our Ron must be smaller than 650Ω. *We should also account for the parasitics of the switch itself as we increase it's width.*

2. With our transistor characterization testbench (while biasing at small triode Vds) we, finnd the minimum width required for our desired value of Ron (we bias the transistor in triode and sweep it's width). In our case, we also found the value where Ron(Cdd+Css) is minimal which was in the vicinity of 1µm, leading to Ron=325.98Ω, and supporting a local oscillator frequency up to 4.88GHz with some room for parasitics. *However, as we shall see later, it is often preferable to size the switches modestly larger for linearity improvements. (our **final device sizes were 8µm at minimum 60nm length**)*

3. Choose Cseries: Cseries is used to block any DC current to be carried by the mixer; it is normally also chosen to resonate with the LNA tank from the previous stage (albeit our LNA is ideal in this case). For our Cseries capacitors, we chose a large integrateable value on-chip of 500fF (also based on [4], [5]).

4. Choose a differential filter at the output of the mixer. At this point in the receiver chain, we are operating in baseband frequency hence we can utilize a capacitor placed differentially to remove high frequency noise due to charge injection and clock feedthrough effects. We choose a value of 2pF (integrateable on-chip).

5. Next we choose the necessary values for the "ideal" transimpedance amplifier to set our desired bandwidth and gain (first iteration). In our case and assuming a nominally 40uA (transduced from -50dBm input power) single ended peak current and given a supply of 1V, our maximum resistor is 25kΩ and correspondingly for a bandwidth of 2MHz Cf=3.183pF.

V. TIA Implementation

The transimpedance amplifier design for passive mixers can be implemented with either a common-gate-based design or an opamp-based design. The Opamp-based design is most common and has the advantages of presenting a very low input impedance to the mixer and supporting a large swing at the output [4], [5]. We opted for the design of a folded cascode Opamp implementation given it's ability (due to the wide-swing current mirrors) to operate under low voltage supplies. Additionally in order to obtain the largest gm per Id from our input NMOS differential pair we operated them under subthreshold and sized them modestly large. The design procedure for the folded cascode Opamp was:

1. From the bandwidth and capacitive load calculate necessary gm of input pair $gm = w_{ta} x C_{load}$

2. Calculate Id and sizing needed for input devices. (from gm)

3. Calculate branch bias current based on input pair Id requirements. (allocate less or equal to 20% to folded output stage)

4. Enforcing Veff~120m find transistor sizes from respective Id.

5. Determine Vb1 and Vb2 bias voltages, to maintain wide swing cascode transistors in saturation.

5. Design the common-mode feedback circuit to enforce an stable output common-mode set-point voltage.

6. Assess the intrinsic gain and ft of the opamp (intrinsic gain must be larger than closed-loop gain (30dB for us) and $W_{ta} > A_{cl} x W_{t\_ol}$ i.e. Ft must be larger than ~400MHz. For our designed Opamp ($A_{ta} = 48.48\, dB$ $f_{ta} \sim 900\, MHz$, dominant pole compensated)

7. Assess the open-loop response of the opamp to assess bandwidth and stability: the open-loop Ft must be greater than 2MHz with sufficient phase margin ($f_t = 54.23\, MHz$ $PM = 86.74\, degrees$)

8. Finally use the closed-loop (actual mixer test-bench) to measure gain and bandwidth response of the circuit to match the required specs.

The final values chosen to yield the desired gain and bandwidth performance were **R'f=4.95kΩ and C'f=16.1pF**

VI. Measurement and Results

The following is the schematic for the folded-cascode Opamp with component values annotated followed by the common-mode feedback circuit utilized. Note the **total power consumption was 315.88μW.** In retrospect, the Opamp designed was over-spec'ed and could have been optimized to save power.

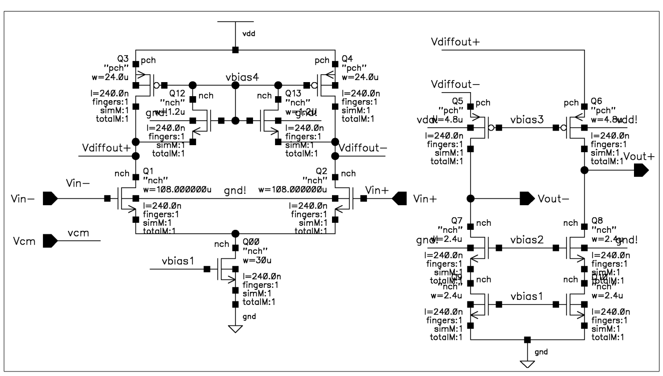

Figure 3: Folded Cascode Opamp (with values)

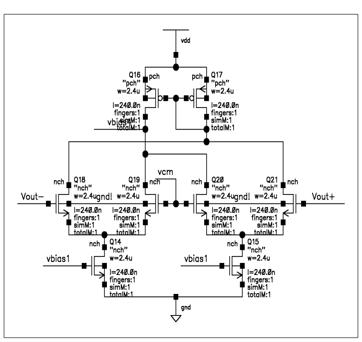

Figure 4: Common-mode Feedback Circuit

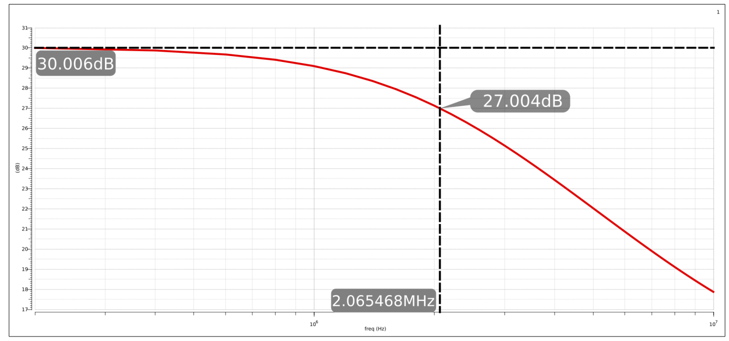

Figure 5: Voltage Conversion Gain vs. RF Freq
Also note bandwidth marker

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Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 3.47303e-05
Total Input Referred Noise = 1.2099e-06
The above noise summary info is for pnoise_usb data
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Figure 6: Integrated IR Noise (100k - 2M)

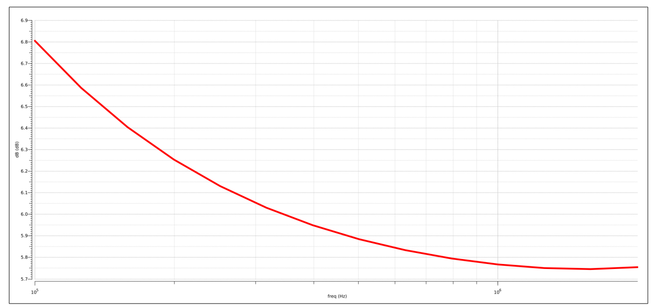

Figure 7: Noise Figure vs. Frequency (supplementary)

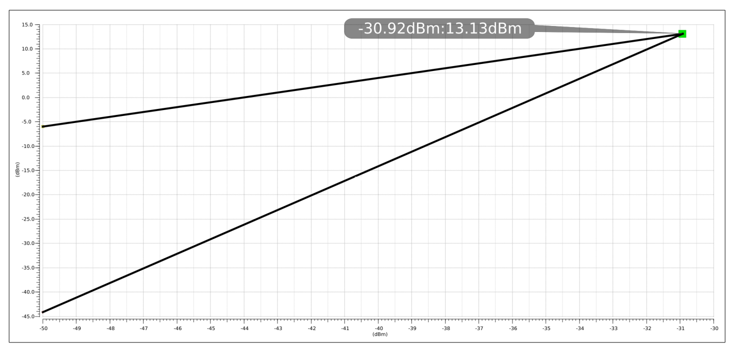

Figure 8: Linearity IP3 (rapid IP3)

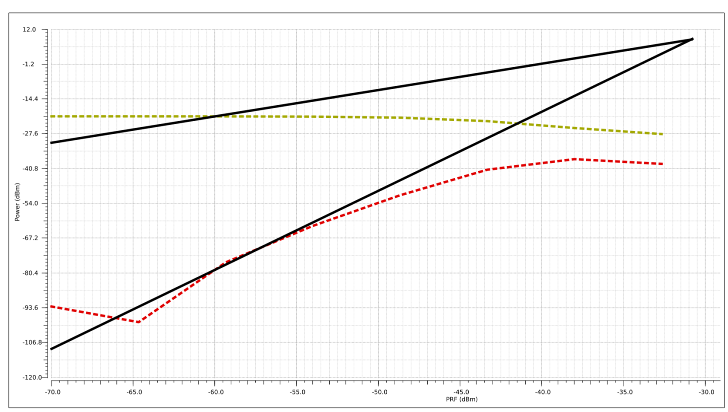

Figure 9: Linearity IP3 (QPSS and QPAC analyses)

Note: it was not specified whether the IP3 linearity was input or output referred (IIP3, or OIP3). Considering the complete receiver gain (not just passive mixer conversion gain), the difference from OIP3 to IIP3 is large (with some error due to chosen extrapolation point), hence referred back to the input, we were unable to achieve an IIP3 figure of 10dB in our case.

References

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[2] Mixer Design Using SpectreRF, Spectre RF Workshop: https://filebox.ece.vt.edu/~symort/rfworkshop/Mixer_workshop_instruction.pdf

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[4] Analysis and Optimization of Current-Driven Passive Mixers in Narrowband Direct-Conversion Receivers: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5256993

[5] A 1.1-mW-RX 81.4-dBm sensitivity CMOS transceiver for Bluetooth low energy: https://www.researchgate.net/publication/258793567_A_11-mW-RX_814-dBm_sensitivity_CMOS_transceiver_for_Bluetooth_low_energy