LNA Design

***Abstract* – This assignment paper presents a low-power narrow-band LNA intended for use in 2.45GHz ISM band applications. The LNA is designed in a 65nm CMOS technology and achieves the desired requirements while consuming 372µW.**

Index Terms – Low power, LNA, 2.45GHz, ISM

I. Introduction

The performance requirements for the single-ended, voltage-mode LNA are, in order below:

Center Freq. Fc (GHz)	-3db Bandwith BW (MHz)	50 Ω Input Matching S11 (dB)	Gain (dB)	Linearity IP3 (dBm)	Noise Figure NF (dB)	Power (uW)
2.45	100	< 10	20	> -15	< 5	< 500

The following sections will be covered in this paper: (II) Topology selection, (III) Circuit intuition/understanding, (IV) Design procedure, (V) Simulation and optimization process (VI) Results and discussion.

II. Topology Selection

After reviewing lecture material, the reference textbook chapter on LNAs and a brief research survey, it quickly became clear that a major driving constraint for this design would be power consumption followed by the narrow-band operation. Two options emerged as potential candidate topologies: (1) the complementary common-source with L-matching network – interesting due to low-supply operation and current-reuse – and (2) the common-source inductive degenerated LNA – best performance/power tradeoff for narrowband designs; We decided to start with the CS inductive degenerated LNA as our first candidate.

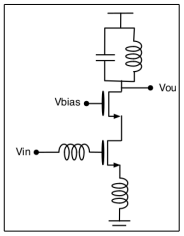
III. Circuit Intuition/Understanding

Initially, we would like to match the input impedance of our LNA with the real 50Ω output impedance of the antenna for maximum power transfer. One way we can accomplish input matching without incurring in the thermal noise of resistors is through the use of active devices. Unfortunately, looking into the gate of a MOSFET we have an inherent gate capacitance (Cgs), I.e. an input reactance we would like to cancel – resonate – at our desired center frequency. *We can thus introduce a inductive component at the source of our amplifier to achieve this purpose.*

We can then calculate the input impedance looking into the gate as (small-signal simple model): $Zin=\frac{V_g}{I_g}=(V_{gs}+I_s S L_s)$ where $V_{gs}=\frac{I_g}{SC_{gs}}$ and $I_s=I_g+gmV_{gs}$ substituting expressions we get: $Zin=\frac{\frac{I_g}{SC_{gs}}+S(I_g+gm\frac{I_g}{SC_{gs}})L_s}{I_g}$ subsequently dividing through by Ig, expanding and canceling: $Zin=\frac{1}{SC_{gs}}+SL_s+\frac{gm}{C_{gs}}$ and factoring $Zin=\frac{L_s gm}{C_{gs}}+S(\frac{1}{S^2C_{gs}}+L_s)$ substituting s = jw and expanding $Zin=\frac{L_s gm}{C_{gs}}+jw(L_s+\frac{1}{(jw)^2C_{gs}})=\frac{L_s gm}{C_{gs}}+j(wL_s-\frac{w}{w^2C_{gs}})$ Finally we have our **Zin:** $Zin=\frac{L_s gm}{C_{gs}}+j(WL_s-\frac{1}{wC_{gs}})=R_{in}+j(X_{ls}-X_{cgs})$ A very interesting result and hence the importance of this circuit: *the input impedance of a common-source stage with inductive degeneration is composed of: a purely resistive component Rin and a reactive component (Xls – Xcgs).*

I.e. **Rin:** $Rin=\frac{gmL_s}{C_{gs}}$ and **Xin:** $Xin=X_{ls}-X_{cgs}$ where $X_{ls}=wL_s$ and $X_{cgs}=\frac{1}{wC_{gs}}$

The input resistive component is very interesting, it gives us the freedom to manipulate Rin through the transistor gm, the degeneration inductor and our gate capacitance. Surprisingly, note that $w_t=\frac{gm}{C_{gs}}$ is the transition frequency of our transistor, seeming to indicate that we may "benefit" from operating with very slow transistors, or conversely very small inductances (either of which we can use to our advantage, either to reduce power consumption or to reduce area respectively). However we still have to deal with the additional reactive component existent for Zin, ideally we want them to resonate (cancel out) at our target resonance frequency. Ideally we would want: $Z(w_c)=j(w_cL_s-\frac{1}{w_cC_{gs}})=0$ Now, unfortunately at frequencies of interest: $w_cL_s\neq\frac{1}{w_cC_{gs}}$ (it is hard to match the reactive terms to cancel each other at our desired center frequency). Hence, normally in practice, an additional pad capacitance is considered (in order to add more freedom in setting Rin) and an off-chip larger inductor is added in series with the gate to resonate with Cgs to allow for canceling reactive components of Zin at Fc.

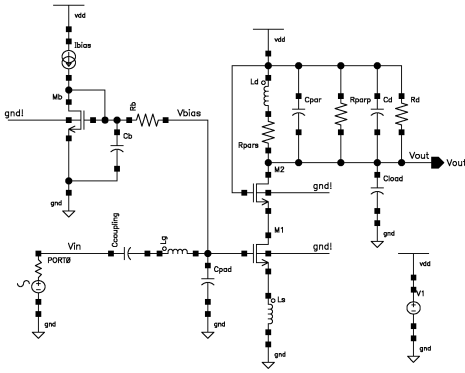


The cascode device is used for isolating the input match bias network (otherwise we would have to account for the Cdg miller cap of our transconductor amplifier)

The load is designed as an LC tank which ideally presents an open-load (max gain of common-source: gm x rds) at resonance.

IV. Design Procedure

Our full inductive degenerated common source LNA topology with cascode and LC tank load. (bias network on the top left)



Note:
Ld modeled with parasitics

Rd is used to limit our gain

Cload is the in-capacitance of next stage

1. Device characterization: perhaps the most important step in the design process is characterizing and biasing your device to give the best performance per power consumed, in our case:

a. Plot of gm/Id versus device width: helps us find the nominal device dimensions with largest transconductor gain efficiency.

b. Plot of gm vs. Id for the nominal device (sweeping Vgs): here you will find the maximum gm the device can give you for a given current. Normally gm reaches a plateau at highest currents (marginal returns), so we bias at 0.8, 0.9 of max gm and we also limit current to ¾ or less of our total budget (to allow for other bias currents).

c. Sweeping multiplier size (constant current point): Widening the device (to a reasonable limit) while keeping our bias current (adjusting Vgs) allows us to get a little more gm for our given drain current.

From our simulations, our transistor bias point used (edge of subtreshold): Wnom=660n, **Lmin**=60nm, **M**=20, **Ids**=320uA, **gm**=5.051mS, gm/Id=15.79/V, Cgg=10.39fF, Vth=403.5mV, Vov=-134.4uV, Ft=77.45GHz. Furthermore, we are assuming the use of a bondwire inductor at the source **Ls**=1nH.

2. Calculate Rin: and add to Cpad to yield Rin=50Ω

Assuming a bond-wire source inductor (Ls), The resistance looking into the FET without any additional "pad" capacitance (only gate capacitance): $Rin_{FET} \simeq W_t x L_s = 486.14\,\Omega$ where $W_t = \frac{gm}{C_{gg}} = 4.86X\,10^{10} rads/s$ $F_t = 77.37\,GHz$ thus for Rin=50Ω we need to add additional lumped pad capacitance of: $C_{pad} = \frac{gm\,L_s - R_{in} C_{gg}}{R_{in}} = 90.63\,fF$ leading to $C_{g\_total} = 101\,fF$

3. Calculate Lg: to resonate canceling input reactive components
We want to enforce $Z(w_c) = j(w_c L_s + W_c L_g - \frac{1}{w_c C_{g\_total}}) = 0$ for this to follow, we choose $L_g = \frac{1}{w_c^2 C_{g\_total}} - L_s = 40.77\,nH$ (also from eq 102 in textbook): This will be our off-chip inductor.

4. Cascode device: The cascode device dimensions are chosen equal to the input transistor. (for backward isolation)

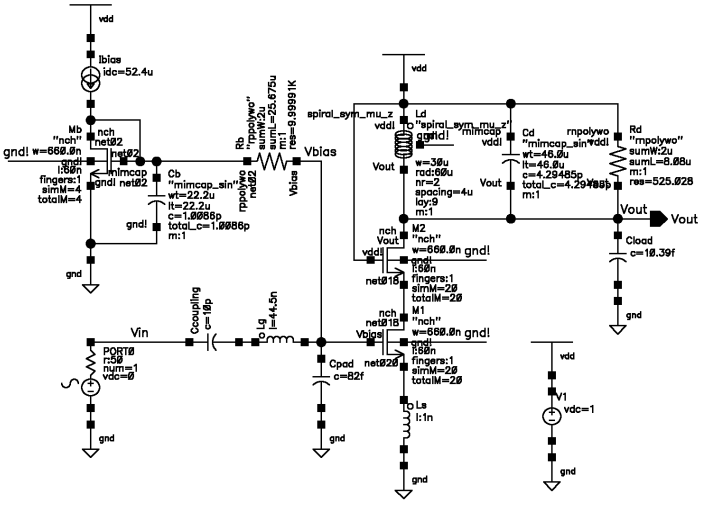
5. LC tank calculation: Ld and Cd to achieve resonance at Wc
Now we ought to select the value of Ld (and additional Cd) such that it resonates with the total capacitance at the drain node. (including Cdb, Cdg, input capacitance of next stage and inductor's parasitic input capacitance).
Starting from the assumption of **Ld**=10nH (approx largest inductance for 65nm) and its parasitics from the book, we find the total capacitance needed at the drain node: $C_{d\_total} = \frac{1}{w_c^2 L_d} = 422\,fF$ and thus the extra capacitance we need to add in the tank: $C_d = C_{d\_total} - C_{in\_next} - C_{par} = 378.8\,fF$

6. LNA Gain and Q Calculation: Rd for the necessary gain and Q
Our gain is governed by $A = \frac{R_d}{2\,L_s\,w_c}$ For our desired precise 20dB gain: $R_{d\_total} = 2\,A\,L_s\,w_c = 308\,\Omega$ and $R_d = 322.3\,\Omega$ This is however non-optimal for our necessary narrow-band Q factor $Q = \frac{F_c}{\Delta F_{bw}} = 24.5$ leading to a poor value of $Q = R_{d\_total}\sqrt{C_{d\_total}/L_d} \approx 2$ (see simulation and optimization section for details and updated values below)

7. Design of Bias Network: to bias transconductor in op. point
Following the book guidelines, we chose the bias transistor and bias current about 1/5 the size of the M1 amplifier and drain current respectively. subsequently Rb was chosen to isolate input from bias circuit noise (**Rb**=10kΩ), and Cb was chosen to bypass most of the noise of Rb (at Wc) to ground. (**Cb**=1pF)

V. Simulation and Optimization Process

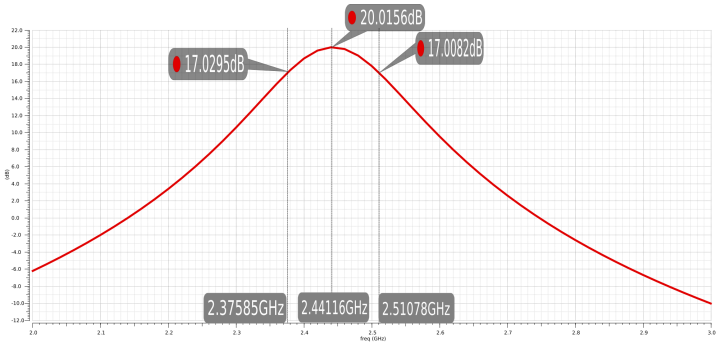
Our results were close to our hand-calculated values requiring some minor parametric optimization of component values (for input matching and gain). Slowly then, we started replacing to on-chip components where applicable. A very important component to increase our narrowband Q factor, was the on-chip inductor. Indeed **our choice of a large value inductor limited the max Q factor**, a better design choice was to choose a small inductor with maximum Q factor (Q=18.3) and compensate by adding a larger capacitance in parallel, i.e. by choosing **Ld**=1nH, then our calculated Cd=4.18pF and Q=20. (closer to our needed Q of 24.5).
The final schematic with updated component values:



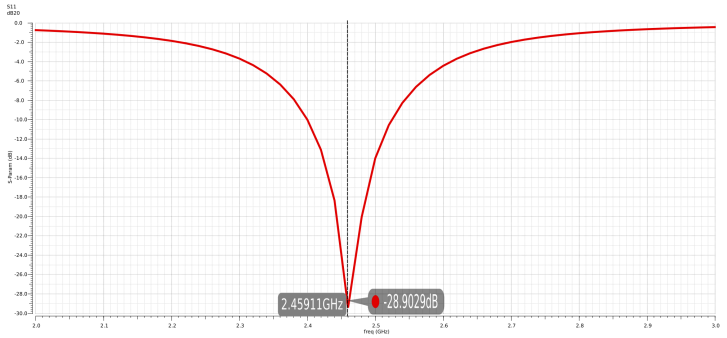
VI. Results and Discussion

The total current consumption was measured at 372.2μA from a 1V supply. Markers in plots below have been expanded to be made visible.

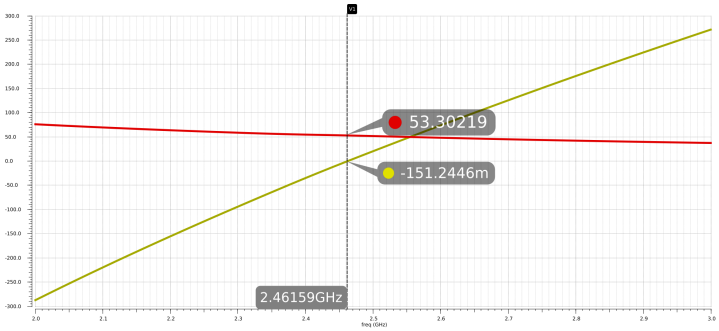
Gain and Fc: 20.016 dB at **2.441GHz Bw=134.93MHz**



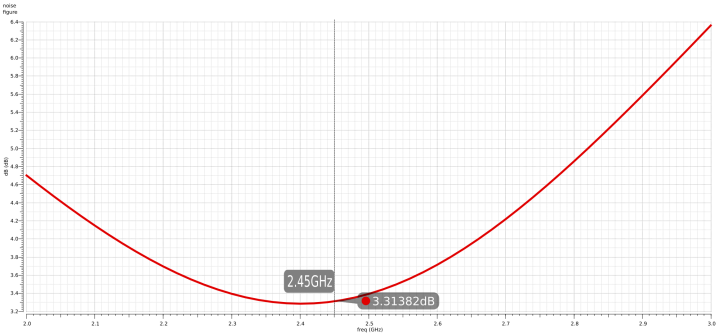
S11 Input Matching: -28.9dB



Zin: Real and Imaginary components (Rin 53.302, Xin=-151m)



Noise Figure: 3.314dB



Linearity (IP3): -13.48dBm

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