Part 1

For part I, we are asked to design a ring-based VCO with the following specifications:

Output Phases:

- 2 quadrature differential outputs (often useful for RF transceivers image rejection)

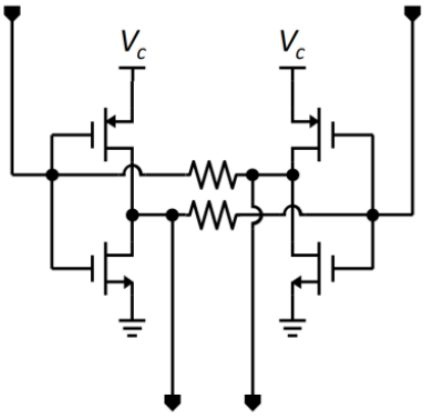
Frequency Tuning Range:

- Minimum 4-8GHz range
- Vcontrol provided by varying supply voltage: 0.5 to 0.8V

Buffer Stage

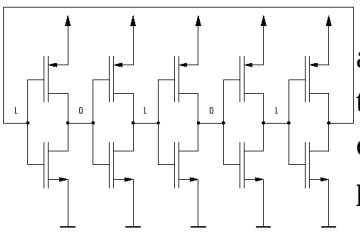
- Output buffers required at quadrature ouputs of ring oscillator
- Capable of driving 20fF load (per side of differential output) over frequency range.
- Capable of maintaining 1Vpp-differential output over frequency range

A. For the implementation of the pseudo-differential inverter we utilized the topology outlined in the assignment write-up, mainly:



If we treat the following topology, as a digital circuit approximation i.e. if we assume switches spend the majority of their time either in triode or cutoff, we can use the simpler model for the transistor switches governed by the ON resistance (during triode), and the effective capacitance (due to the lumped gate and drain capacitances of the switch). Hence in this case we can approximate: $R_{on} \propto L/W$ and $C_{eff} \propto W\,x\,L$

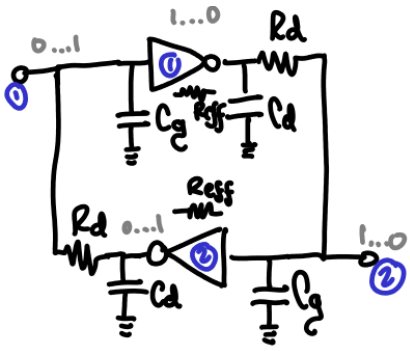
(In digital circuits we benefit from the scaling of feature – length – sizes). we rely on these intrinsic parasitic resistive and capacitive components of the switch to define the intrinsic RC constant of the switch and hence the inherent speed of the technology. In the case of the standard ring oscillator model we treat each inverter as a delay cell with its propagation delay governed primarily by this switch RC constant. In the simplest model then, the oscillation frequency then depends only on the propagation delay of each inverter cell and the number of stages used for the oscillator. *Note for sustained oscillation, the minimum number of stages in the ring is governed by the necessary phase shift around the loop and the gain of each cell must be unity or larger at the desired oscillation frequency.* Hence we have the simplest model for a ring oscillator. (e.g. 5-stage ring oscillator below)



Here we can control the oscillation frequency by sizing our devices appropriately to yield the desired Ron and Ceff for each cell and hence the propagation delay. (alternatively we can also add explicit capacitances at the output of each inverter to enforce our desired RC propagation delay while keeping our nominal device sizes fixed)

In general for a ring-oscillator: $f_o = 1/T_o = 1/(2xnT_d)$ Where n is the number of stages in the ring and Td is the average rising and falling propagation delay of the inverter (given by the RC constant and logic and supply voltages).

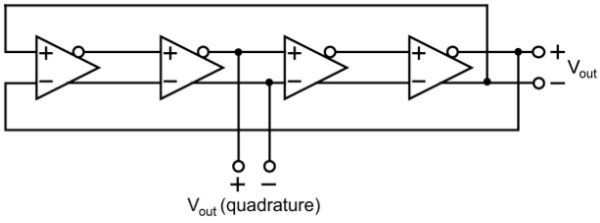
Having this knowledge on hand, we can look at our differential inverter topology above and re-draw it to try to understand it's operation a bit more intuitively. (using our digital model approximation)



Let's follow the inversion logic of this circuit (use Vdd=1 for simplicity):

Initially for a growing small differential input In1>=0.51V and In2 <= 0.49V, Inverter1 starts to pull charge (through Reff) from Cd and Cg (additionally through Rd), similarly Inverter2 starts charging Cd and Cg. The additional path through Rd enables the strong regeneration of the differential logic levels at the inverter inputs (positive feedback). However we must be mindful that at small signal levels the gain of our inverter is given by its intrinsic gain (gm) and its output resistance (ro) which is now also loaded by Rd, hence if we choose Rd to be too small (for the reasons above) the gain at our desired frequency drops below unity and the ring oscillator fails to maintain oscillation.

To build our differential ring oscillator we can then follow the standard topology:



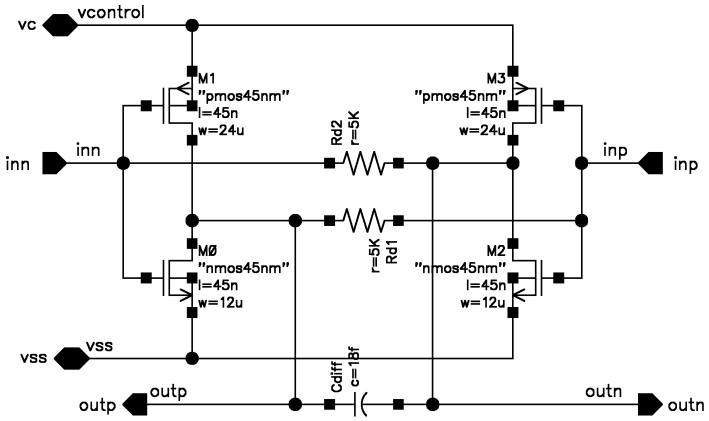
Here every differential inverter introduces a 45 degree phase shift (180 degrees once around the loop satisfies condition for oscillation). Additionally we have a 90 degree phase shifted output available which we can use for quadrature as required.

A viable design procedure starts by choosing the smallest device length allowed by the technology and nominal width (initially we started with roughly W/L: 2Lmin/Lmin) and subsequently find the minimum Rd necessary to maintain oscillation: this yields close to our maximum oscillation frequency attainable at Vdd=800mV (with Rdelay~20k, Fosc_max~10GHz).

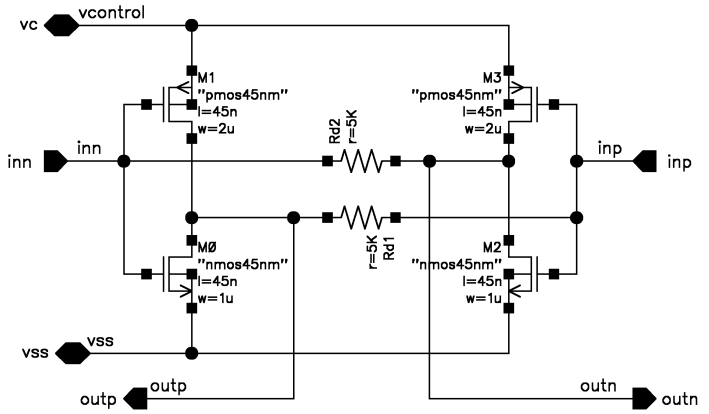
However at lower Vdd=500mV (and reduced current available) our gain is not sufficient to guarantee oscillation (otherwise requiring the use of a large resistor ~200k), an alternative approach is to make our devices much wider and consume more current to (increase gain) guarantee unconditional oscillation and make use of small nominally sized integrateable resistors for Rd. (this simplifies our design substantially)

Next, we needed to aim to optimize the use of our control voltage range to cover the largest range from 4GHz to 8GHz. In our case we added small capacitors at the output of our differential ring inverters to give us finer control and reduce our oscillation frequency at the higher end closer to 8GHz. (we can also reduce these capacitance values at the nodes connected to our output buffers to present equal capacitive loading to each stage without modifying device sizes)

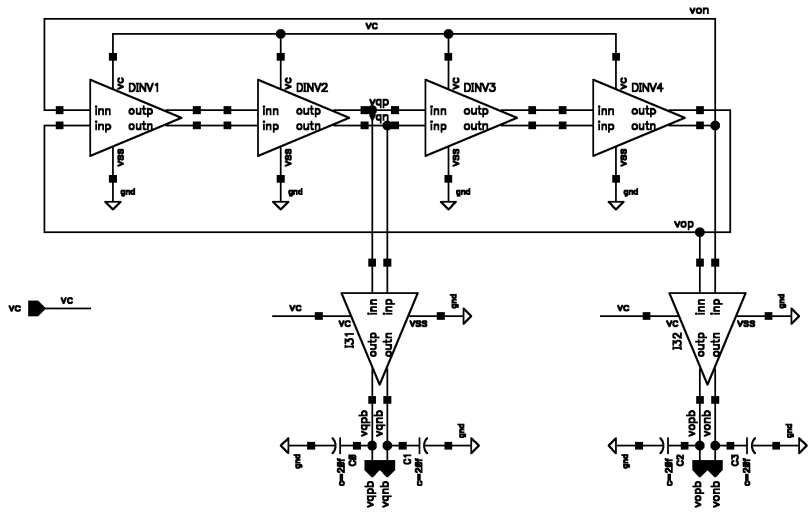
B. The following is our differential inverter with annotated device sizes:



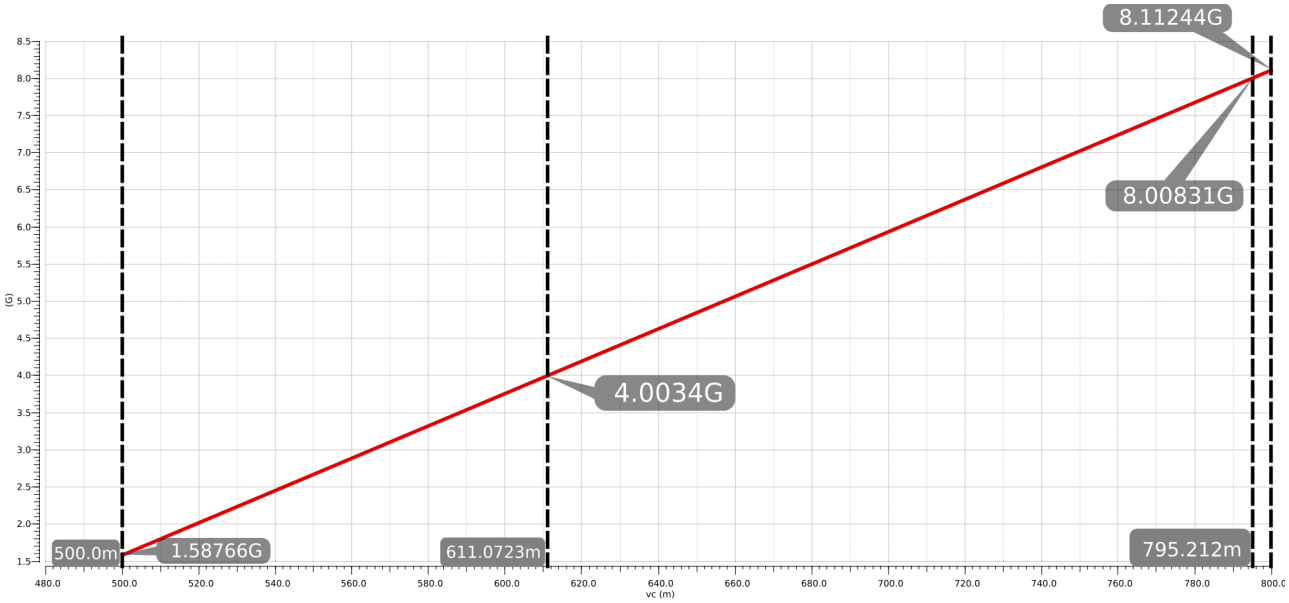
We re-used the same differential inverter topology for our buffers (digital) but utilizing the minimum dimensions necessary (to present the least capacitive loading to the ring oscillator) to be capable of driving the 20fF loads at each of their output nodes while maintaining a 1Vpp-differential amplitude (most critical at low Vdd=500mV). From our simulations the minimum device sizes that guarantee this condition was (buffer schematic with device sizes annotated)



And the complete schematic for the ring oscillator:

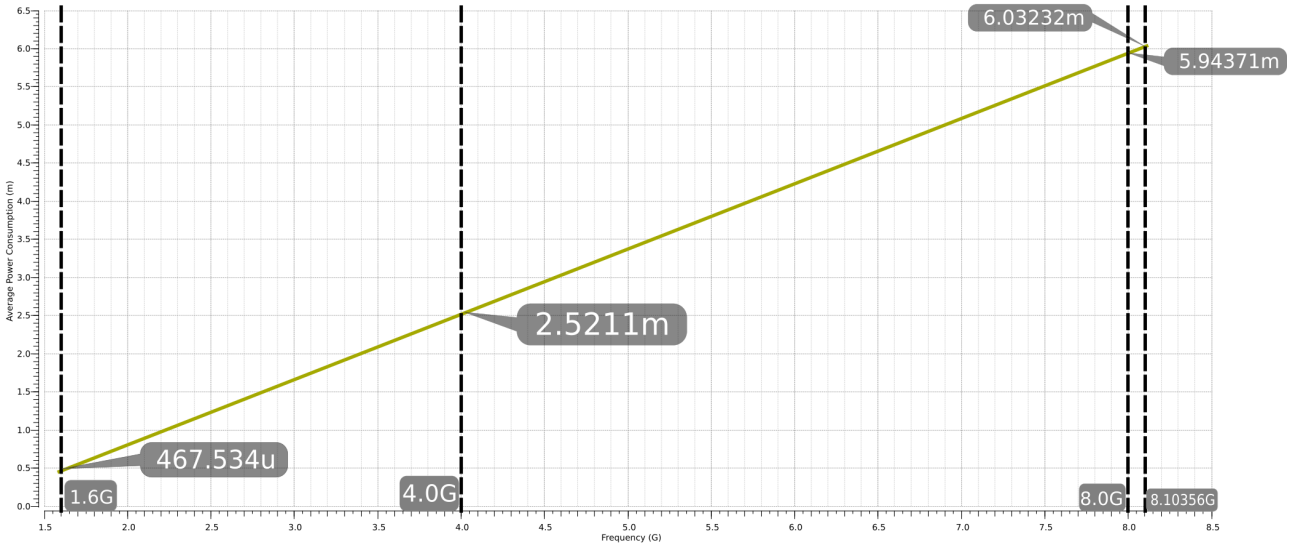


C. The following is the plot of our output frequency vs. supply voltage.

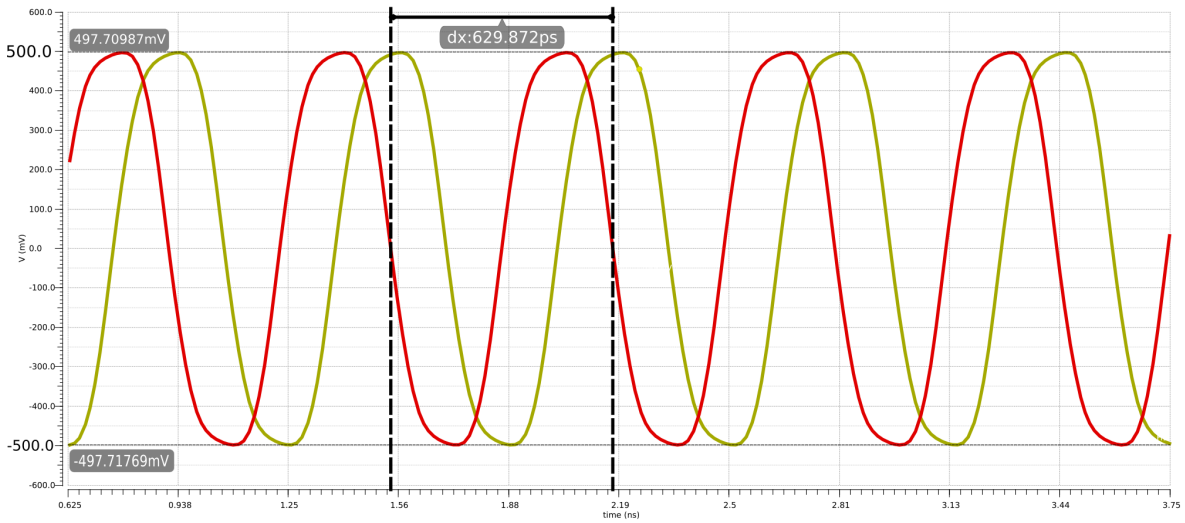


D. The following is the plot of power consumption vs. output frequency

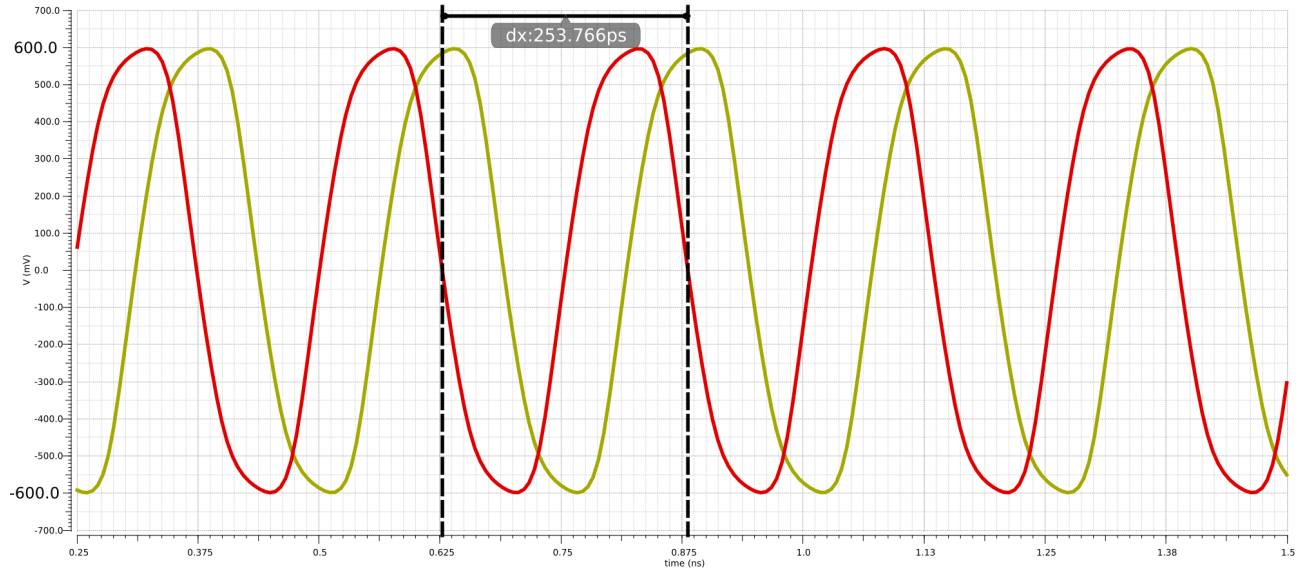
Note the current was calculated from our average current consumption while sweeping Vcontrol.



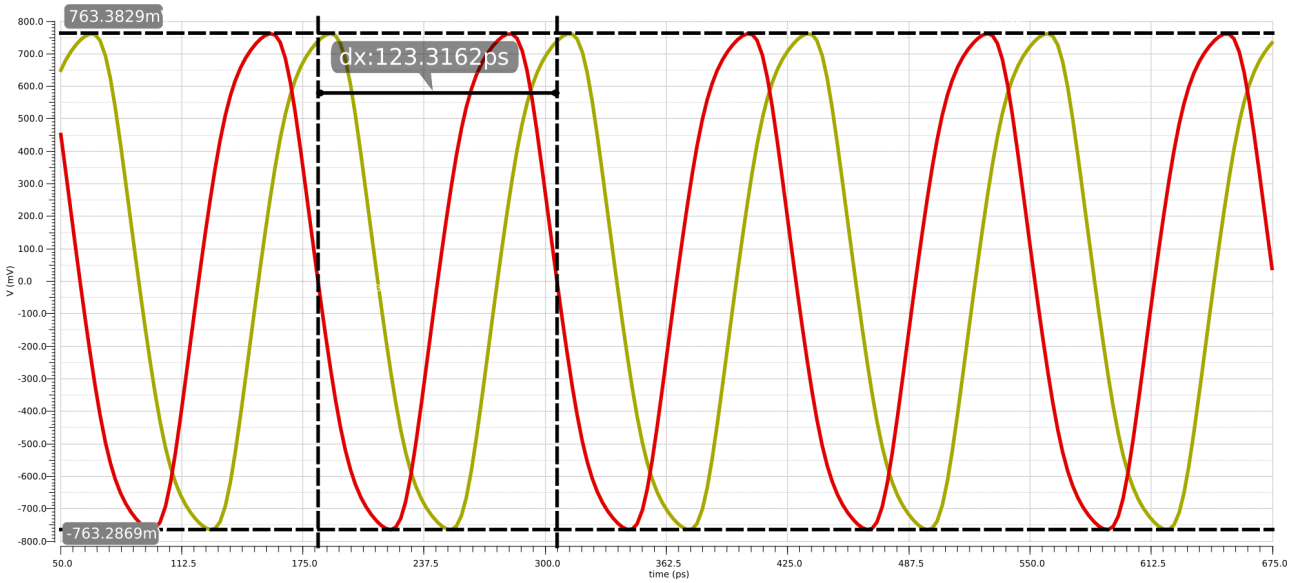
E. The following are our transient simulation results with our quadrature waveforms for both 0.5V and 0.8V cases respectively. **Transient Waveform at Vc=0.5V**



Transient Waveform at 4GHz (Vc=611mV)

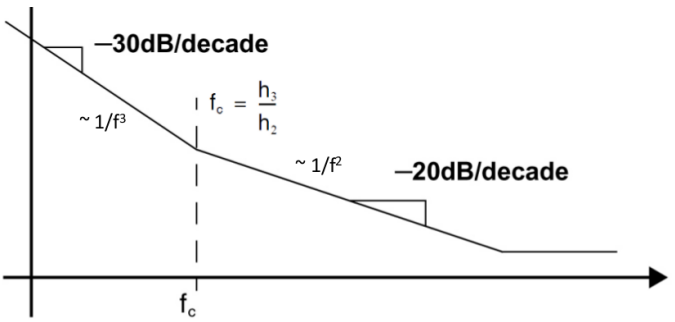


Transient Waveform at 4GHz (Vc=0.8V)



F. The simulated phase noise of our ring oscillator should have the standard oscillator phase noise profile (below for reference)

$$S_{\phi,osc}(f) = h_0 + \frac{h_2}{f^2} + \frac{h_3}{f^3}$$



Where the $1/f^3$ phase noise term corresponds to 1/f flicker noise upconverted by the oscillator.

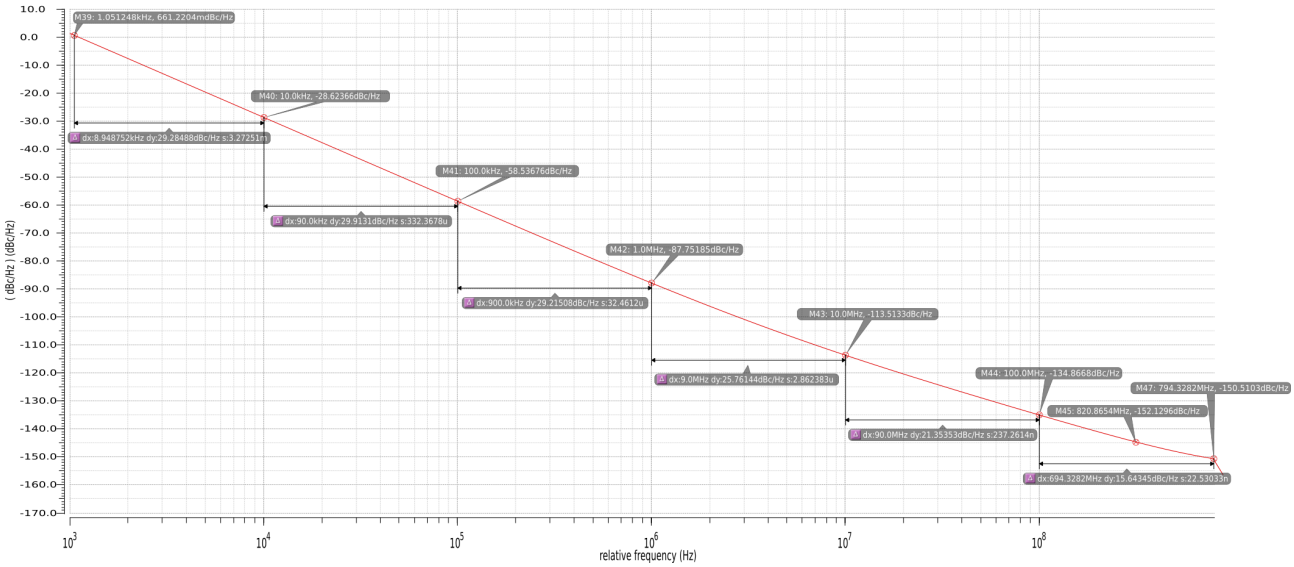
$1/f^2$ phase noise corresponds to white noise upconverted by the oscillator

Finally the h0 term corresponds to white noise at the output of the oscillator.

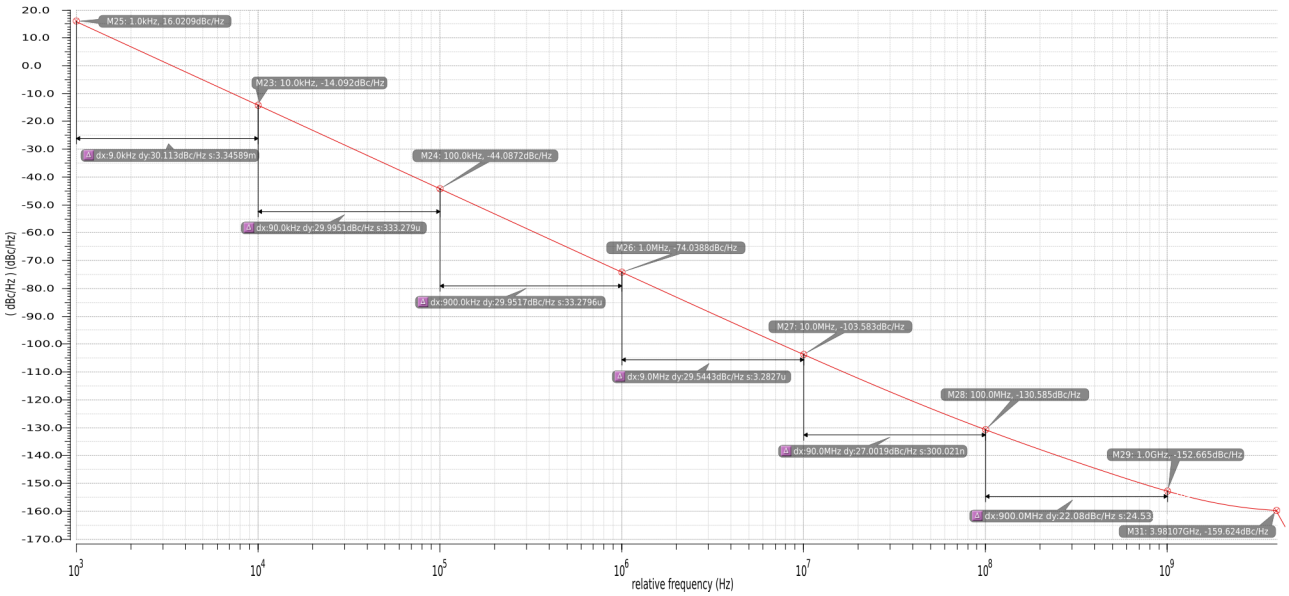
(recall the phase noise plot above is in terms of relative offset from the frequency carrier)

Phase Noise at 0.5V Vcontrol

Note up to 10^7Hz relative frequency the slope is -30dBc/decade ($1/f^3$), afterwards the slope turns to -20dBc/decade ($1/f^2$) and finally it can bee seen the waveform starts to converge to h0.



Phase Noise at 0.8V Vcontrol



Note the phase noise power-law model in dBc/Hz is expressed as: $L(\Delta f) = 10\log\left(h_0 + \frac{h_2}{f^2} + \frac{h_3}{f^3}\right)$

To calculate our coefficients (procedure for Vc=0.8V) We know at very large frequencies the white noise component of our phase noise dominates (minimum slope):

$$L(\Delta f \to Large) \simeq 10\log(h_0) \simeq -160\, dBc/Hz \quad \text{Therefore} \quad h_0 = 10^{(-160/10)} \sim 100\, x\, 10^{-18}$$

On the other hand, at very low frequencies the h3 ($1/f^3$) term dominates (evaluated at 1KHz offset where -30dBc/Hz is prominent):

$$L(\Delta f \to 1\,KHz) \simeq 10\log\left(\frac{h_3}{1\,KHz^3}\right) \simeq 16\, dBc/Hz \quad \text{Hence} \quad h_3 = 10^{((L(1\,KHz) + 10\log(1\,KHz^3))/10)} = 39.811\, x\, 10^9$$

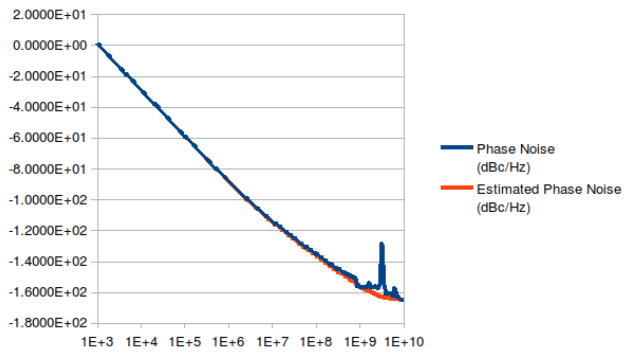
And for relatively large frequency offsets the term h2 ($1/f^2$) dominates (evaluated at 1GHz where we can see a slope of -20dBc/decade)

$$L(\Delta f \to 1GHz) \simeq 10\log\left(\frac{h_2}{1\,GHz^2}\right) \simeq -152.665\,dBc/Hz \quad \text{therefore}$$

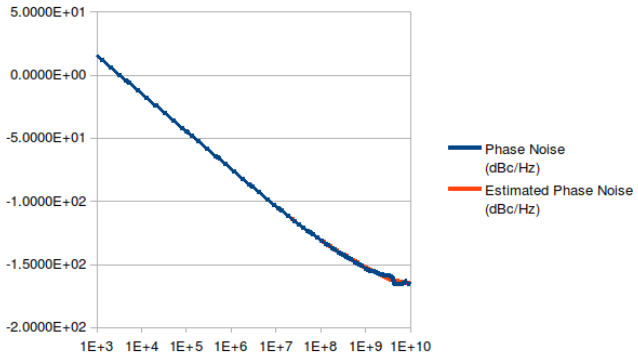
$$h_2 = 10^{\left((L(1\,GHz)+10\log(1\,GHz^2))/10\right)} = 541.38 \quad \textit{The procedure is exactly the same for Vc=0.5V.}$$

Exact coefficients for our phase noise models for 0.5V and 0.8V were then tabulated in a spreadsheet, and then using the phase noise power-law model were plotted overlaid on the original results from our phase noise simulations. (see both plots below)

Phase Noise Model at Vcontrol=0.5V



Phase Noise Model at Vcontrol=0.8V



Part 2

A. In part 2 of the assignment we are asked to design a voltage regulator with an input unregulated supply voltage of Vdd=1.8V. We need to generate a clean regulated voltage varying from 0.5V to 0.8V which will be used as the supply and control for our ring oscillator. The complete specifications are as follows:

Load	Ring Oscillator from part 1)
Supply Voltage (V_{DDH})	1.8V
Reference Voltage (V_{ctrl})	From 0.5V to 0.8V
Regulated output (V_c)	From 0.5V to 0.8V
Maximum C_{DEC}	50pF
Phase Margin for 0.5V < Vcntl < 0.8V	75°
Low Freq (10kHz) PSRR	-40dB
Worst Case PSRR from 10kHz to 10GHz	-10dB

In the design of our regulator we have two main choices: (1) we can use a low-dropout voltage regulator (LDO) or we can employ a standard (non-ldo) linear regulator.

Normally LDOs (1) find applications in low-power designs requiring drops from Vdd to Vreg of a couple of hundred mV at most (200 to 400mV is typical with 100mV being about the smallest attainable with good regulation specs). LDOs employ the use of a PMOS pass transistor with the source directly connected to Vdd; this configuration with a PMOS pass transistor is somewhat more involved as VDD ripple modulates directly the Vgs voltage of the transistor and represents a gain path which needs to be reduced to allow for good PSRR. Hence the Opamp needs to be employed in

a negative feedback configuration to provide a common mode signal to that introduced at the source to keep Vgs constant and allow for good supply ripple rejection.

Non-LDO linear regulators (2) are traditionally used in applications where a larger dropout can be tolerated. For non-ldo topologies with standard Vth devices, dropouts of 0.8 -1.2V are attainable with good specs. In this case an NMOS device is used in a source follower configuration with inherent isolation from supply ripple at the drain of the device (if operated in saturation). Non-ldo topologies are the best choice if low dropout is not a necessary requirement.

Can we get away with a traditional simpler Non-LDO linear regulator topology? In our case, the minimum dropout we need to support is 1V (1.8Vsupply – 0.8Vreg) which falls within the application space for non-ldo linear regulators, therefore we decided to explore this topology first as it leads itself to inherently better regulation specs. For non-LDO linear regulators it is critical to reduce the amount of ripple presented at the gate of the NMOS pass transistor. In this case a folded cascode Opamp is a recommended topology as it presents no feedthrough from the supply ripple to the output of the OTA.

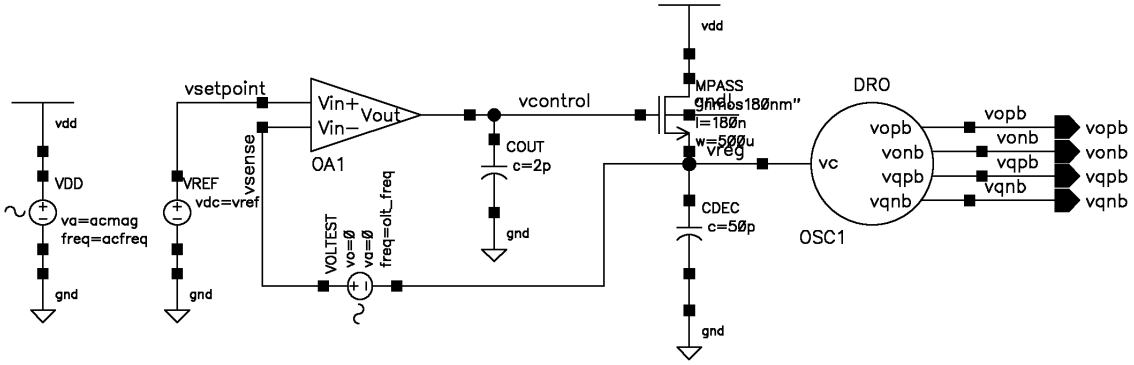
Initially our main concern was whether our folded-cascode OTA could swing to the gate voltage needed to keep the pass transistor over it's threshold voltage – at least Vth plus 0.8V worst case (our hope was to modify our previous opamp design with the specs needed for our regulator). This difficulty is made worse by the fact that the standard pass transistor has it's body/substrate biased to ground but its source is biased at 0.8V thus increasing it's Vth ~650mV.

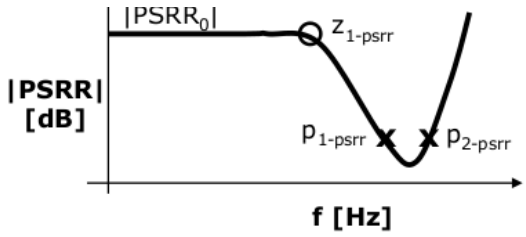
A quick estimate then reveals the rough headroom needed for our top wide swing cascode mirror devices $V_{out\_max} \leq 0.8 + 0.65 \sim 1.45\,V$ therefore we have around 350mV available for both transistors. Initially these transistors are designed around a nominal Veff of 240mV each therefore we had to go back to the design and size and bias our transistors accordingly to reduce their Veff and meet our necessary swing at the output.

In our case we increased the size of the top current mirror to a maximum dimension of 180um to lower it's Veff as much as possible (keeping bias current constant by scaling-up current reference transistor accordingly to keep ratio constant): hence we were able to bias our top mirror devices (in our wide swing current mirror) with a Veff below 100mV. Subsequently we increased the PMOS cascode bias voltage in order to reduce their Veff as much as possible before performance degradation (~150mV Veff). Therefore for our PMOS wide swing current mirror, we operate the uppermost mirror device almost at the verge of entering triode operation (outlined in the reference textbook), leaving more room for the cascode device and allowing the output to swing to our necessary voltage to drive the gate of our NMOS pass transistor. Ultimately we characterized the performance of our Opamp with our open-loop testbench from assignment 2 to be comparable to our past met specifications.

Prior to the use of our implemented Opamp, we employed the use of an ideal testbench: a VCVS ideal Opamp (with dominant pole modeled by rc at the output, and a realistic gain value), our non-ideal pass transistor and an ideal resistive load (Rload~100Ω at 0.8V and ~530Ω at 0.5V) in order to characterize and size our pass transistor in order to lead to practical value for Ron and Vgate drive for our pass transistor (the optimal case for our power transistor was 500um/180nm); then we characterized the PSRR for our regulator under pseudo-ideal circumstances.

B. Using our regulator design testbench below and the class resources for this assignment:



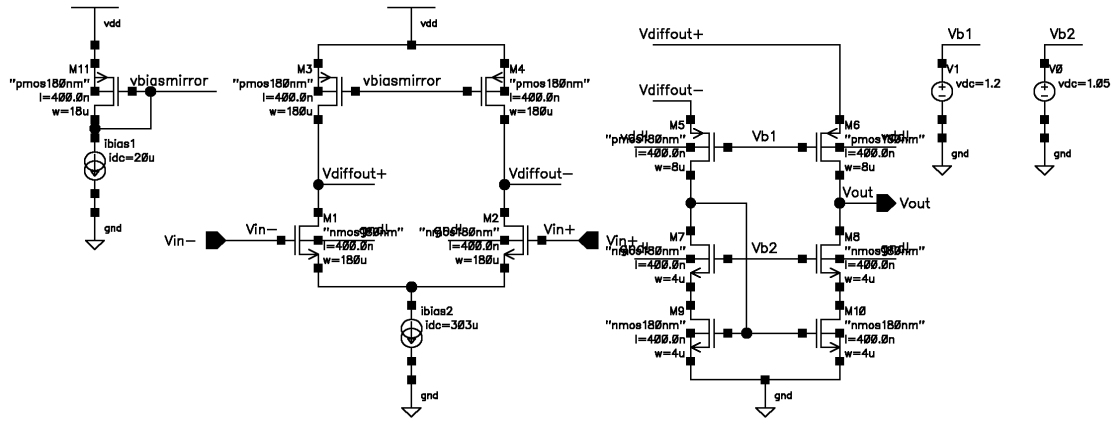


The most important insights in the design of the linear regulator had to do with understanding how the mapping of the PSRR response poles and zeros map to the poles and zeros of the open-loop response of the opamp with feedback network.

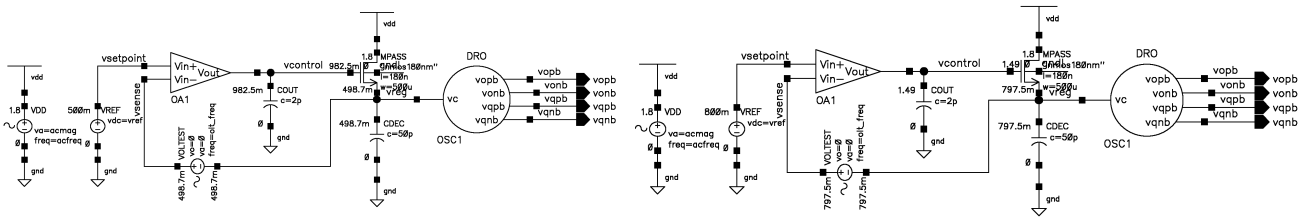
We recognized:

- The low-frequency PSRR is mainly dependent on the intrinsic DC gain of the Opamp
- The P1-psrr pole is almost primarily dependent on the output capacitor Cout (lumped with Cgg) which for our open-loop response (folded-cascode OTA) corresponds to the dominant pole with determines it's 3db bandwidth. It is this capacitor which also contributes to reduce the ripple present at the gate thus improving our PSRR. We set this capacitor to a moderately large value which preserves our PSRR from exceeding -10dB.
- The P2-psrr is dependent on our decoupling capacitor which helps alleviate current ripple introduced at high frequencies. Here we benefit from the largest capacitor we are able to use 50pF.

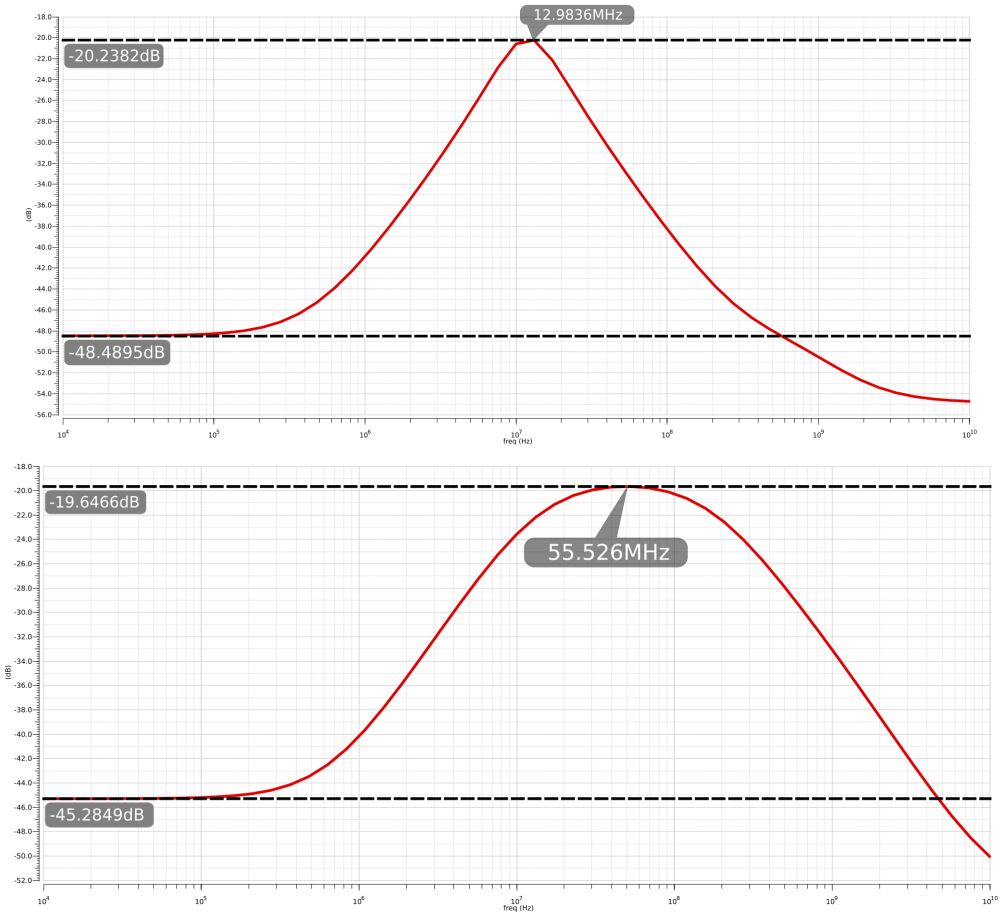
In our case, as long as we can reach our necessary gate voltage for our pass transistor, we will have sufficient DC gain to meet our low frequency PSRR. Then, through the use of an appropriate value of Cout and our decoupling capacitor we are able to meet our PSRR specs over our necessary frequency range. The following is our Opamp Schematic with annotated values:



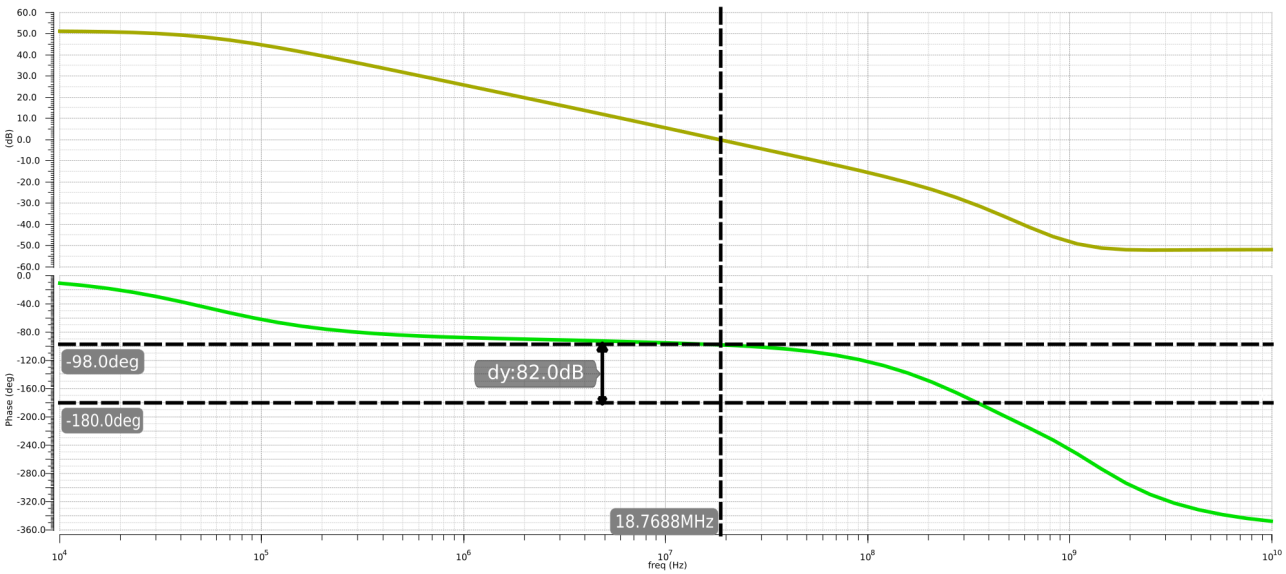
Node Voltages at Vc=0.5V **Node Voltage at Vc=0.8V**

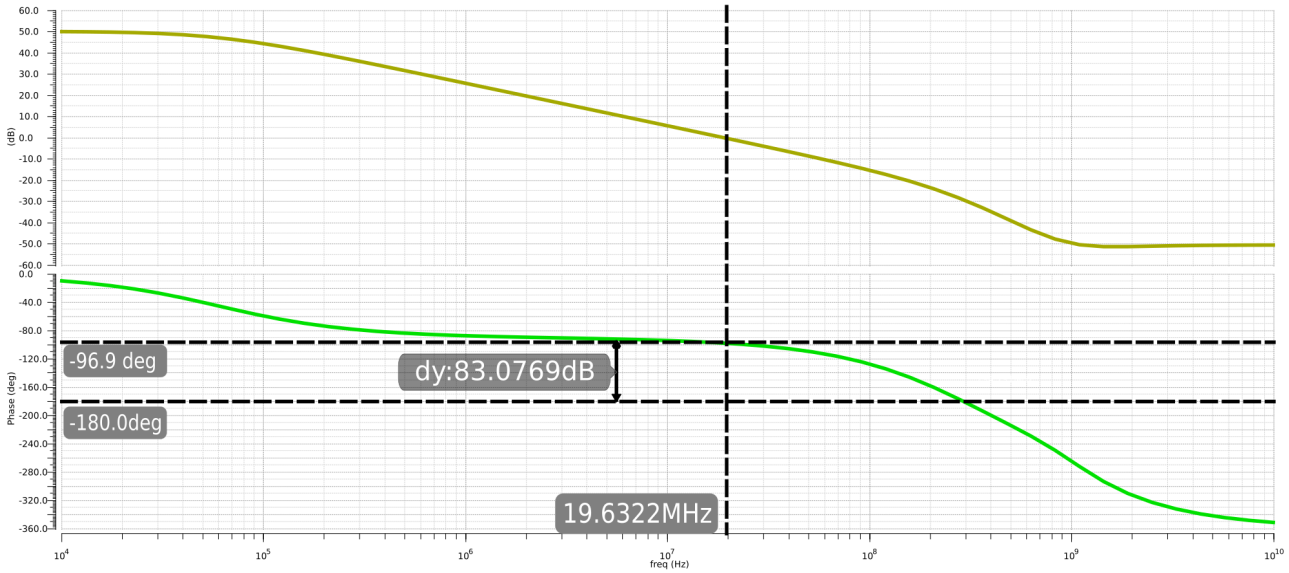


C. The following are the PSRR vs Frequency plots for both Vc=0.5V and 0.8V settings respectively



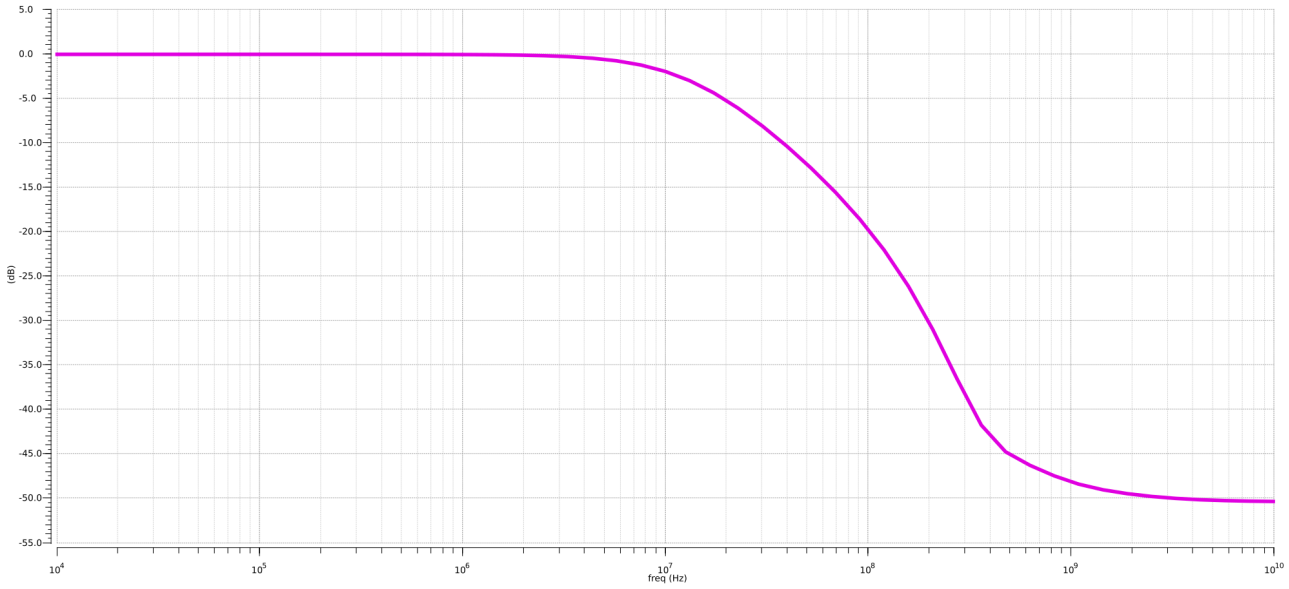
D. The following are AC open loop simulations outlining the phase margin for both Vcntl=0.5V and 0.8V respectively (min PM=82)





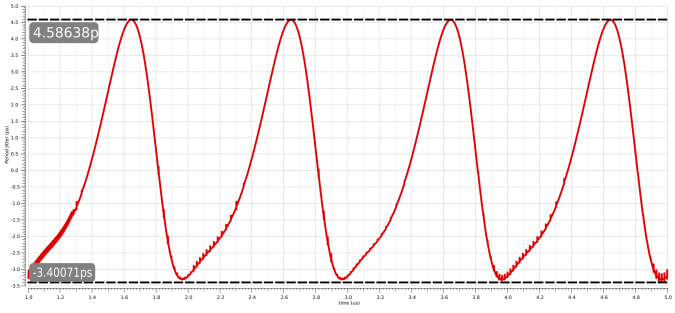
D. The closed-loop AC response from Vcontrol to Vc

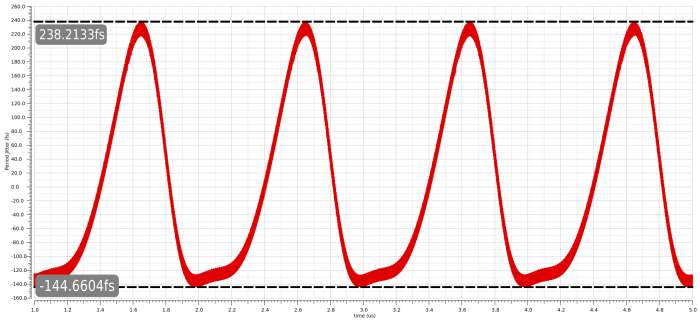
This closed-loop transfer function tells us until what frequency is the feedback loop able to keep regulated Vc in track with our desired setpoint. (after 10MHz, loop can no longer track changes)



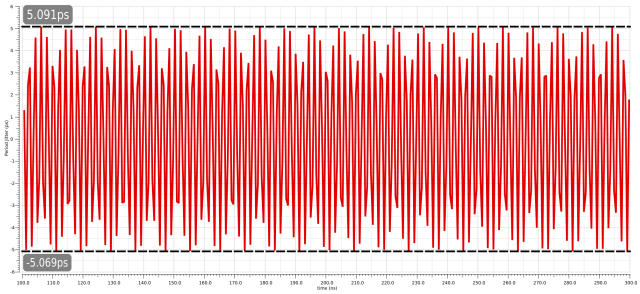
D. The period jitter at the oscillator output (i.e. maximum time deviation from ideal period) under 100mVpp sinusoidal noise applied at our unregulated supply at 1MHz and 500MHz respectively.

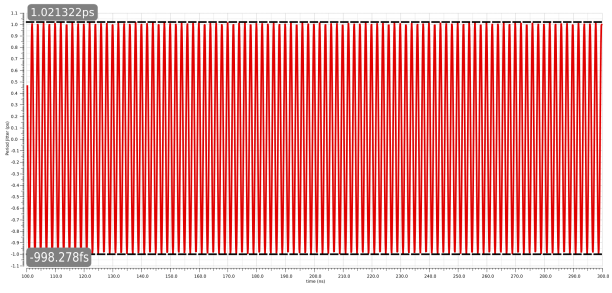
Period Jitter At Vc=0.5V (1MHz supply noise), Period Jitter At Vc=0.8V (1MHz supply noise)





Period Jitter At Vc=0.5V (500MHz supply noise), at Vc=0.8V (500MHz supply noise)





Part 3: PLL Design

For this part of the project we are asked to design an integer-n PLL with the following specifications: $f_{ref}=80\,MHz$ $f_{3db}=5\,MHz$ $PM\geq 60\,degrees$ $f_{clk}=6\,GHz$

Note from our previous VCO design we can calculate our KVCO:

$$Kvco=\frac{\Delta f}{\Delta V}=\frac{2\,x\,\pi(8\,GHz-4\,GHz)}{786.7409\,mV-611.4694\,mV}=\frac{2\,x\,\pi\,x\,4\,GHz}{175.27\,mV}=143.39\,x\,10^{9}\frac{rad/s}{V}$$

The following was the PLL design procedure following our reference textbook:

1. Calculate the N divider ratio:

$N=f_{clk}/f_{ref}=6\,GHz/80\,MHz=75$

2. Choose Q

We chose Q=0.5 to give us a quick phase lock as well as realistic IC integrateable component values.

3. Choose Loop Bandwidth

In our case we are given the desired loop bandwidth to be: $f_{3db}=5\,MHz$ or

$w_{3db}=31.416\,x\,10^{6}\,rads/sec$

note here f3db is being chosen to be around 1/16th of the reference frequency for stability.

4. Choose Wpll

We choose $w_{pll}=0.4\,x\,w_{3db}=12.566\,x\,10^{6}\,rads/sec$ as recommended for Q=0.5

5. Choose charge pump current

Given our equation $C1=\frac{I_{ch}\,x\,K_{vco}}{2\pi N W_{pll}^{2}}$ we choose a charge pump current to yield realizable IC values for C1 and later C2 (assuming a starting value of C1=50pF, slightly larger to lead to adequate value for C2 later on) $I_{ch}=\frac{C_1\,2\pi N W_{pll}^{2}}{K_{VCO}}=¿$

6. Estimate the location of our Zero

Our zero should be located in the vicinity of $W_z = Q\,x\,W_{pll} = 6.28\,x\,10^6\,rads/sec$

7. Calculate the resistor for our loop filter

The resistor for our loop filter is set by the zero location and C1: $R = \frac{1}{W_z\,x\,C_1} = 3.183\,k\Omega$

8. Choose the loop-filter glitch supression capacitor

Initially, the loop filter glitch suppression capacitor C2 was chosen to be 1/10 of C1 (as recommended for Q=0.5), i.e. C2=5pF. However this led to the phase margin being 56 degrees. (below the required 60 degrees)

Hence in order to give us a slightly larger phase margin we made C2 smaller to push the second pole further. (at the cost of larger glicthes present in the Vcontrol input to our VCO)

To give us our desired 60 degrees phase margin we make C2=3.8pF

A. The nominal values for our PLL design parameters are as follows:

$N = 75 \quad Q = 0.5 \quad W_{pll} = 1.26\,x\,10^7\,rads/sec \quad I_{ch} = 25.95\,\mu A \quad C_1 = 50\,pF$

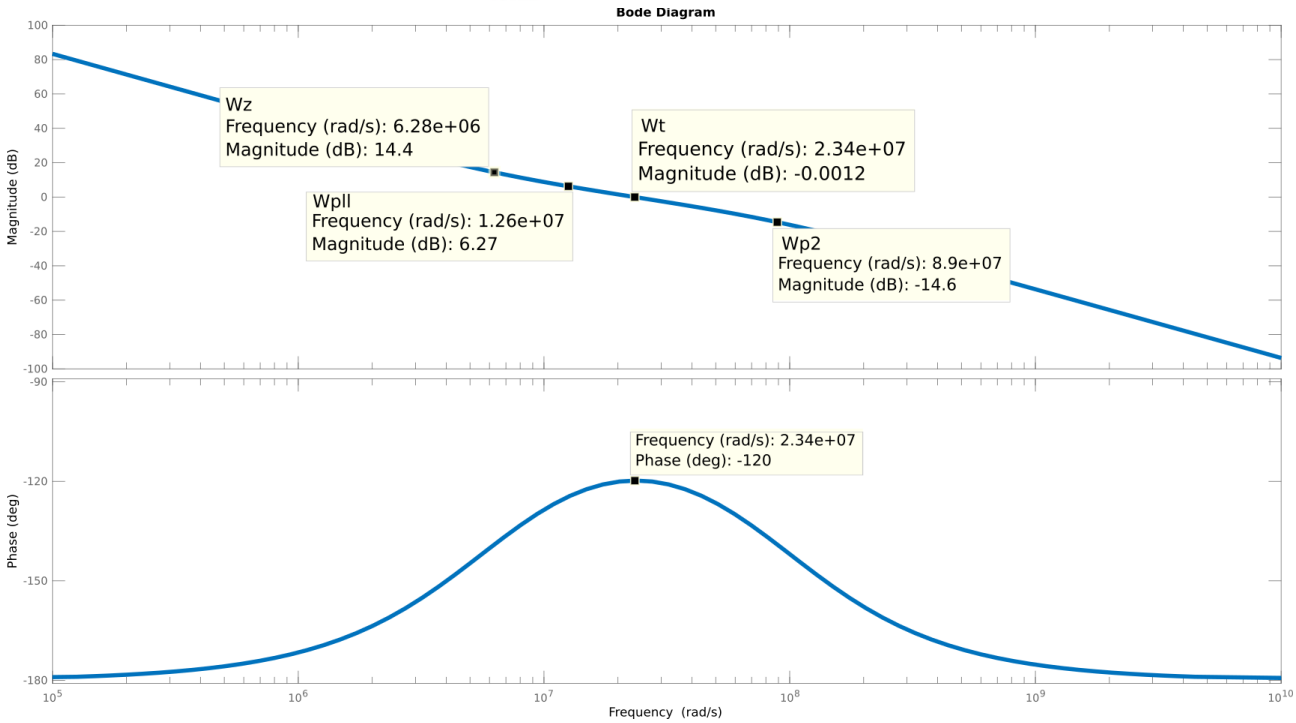
$W_z = 6.28\,x\,10^6\,rads/sec \quad R = 3.183\,x\,10^3\,k\Omega \quad C_2 = 3.8\,pF \quad k_{osc} = 143.39\,x\,10^9\,\frac{rads/sec}{V}$

And we can calculate: $W_t = \frac{W_{pll}}{\sqrt{2}}\,x\,\sqrt{\left(\frac{1}{Q^2} + \sqrt{\left(\frac{1}{Q} + 4\right)}\right)} = 2.26\,x\,10^7\,rads/sec$

B.a Subsequently using the provided matlab plotting script we can plot

Open-Loop Response of the PLL $W_z = 6.28\,x\,10^6\,rads/sec$ where

$K_{pd} = I_{ch}/2\pi$ $K_{ip}H_{ip}(s) = \frac{V_{cntl}(s)}{I_{pd}(s)} = \frac{1}{s(C_1+C_2)} \cdot \frac{1+sRC_1}{1+sR\left(\frac{C_1C_2}{C_1+C_2}\right)}$, and we have our known values for Kosc and N above.



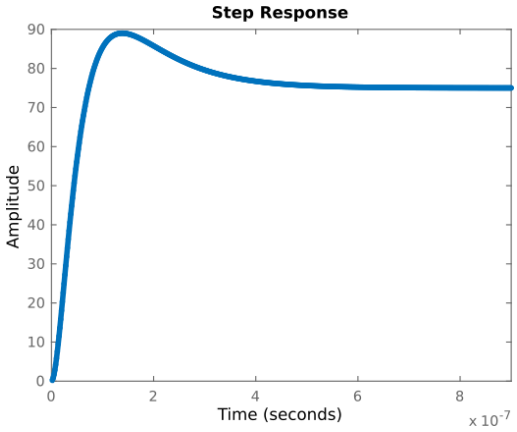
Note here Wt is slightly different as we have moved further the pole Wp2 (for 180-120=60 degrees PM)

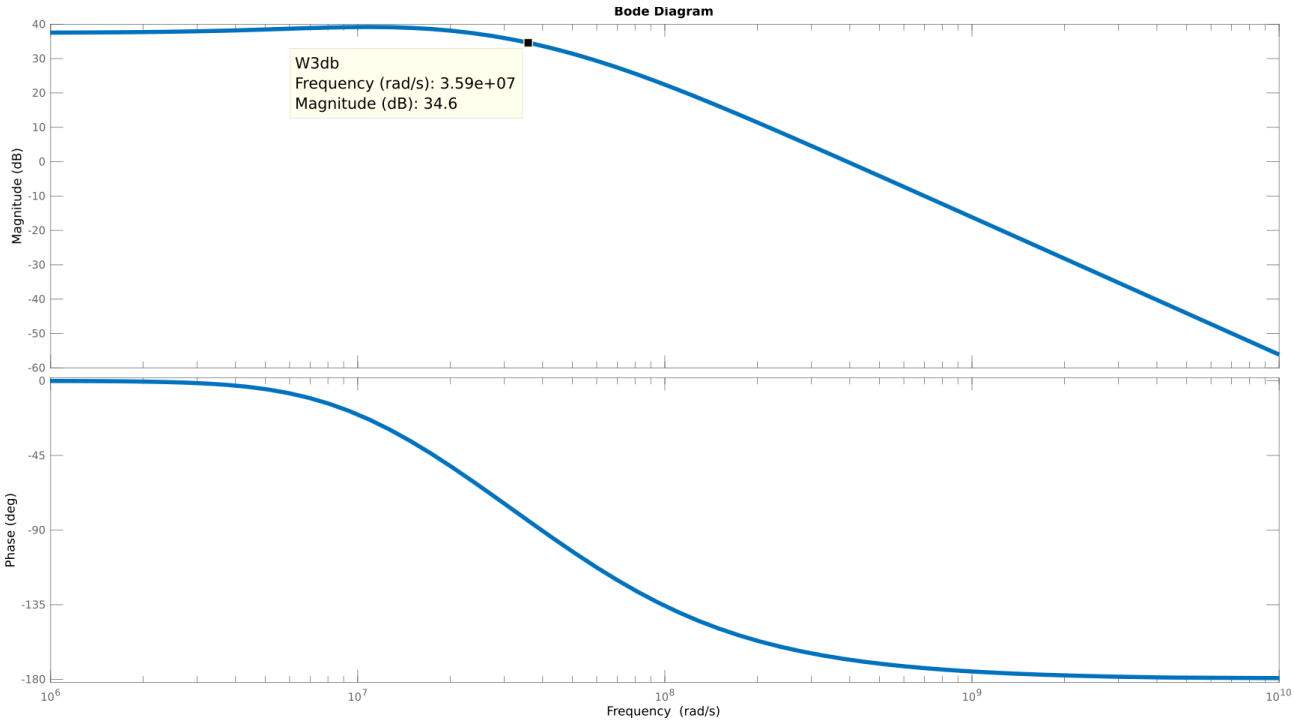
```
Continuous-time transfer function.  (PM = 60.2322)

L(s) =     0.0943 s + 5.925e05

       ----------------------------

       4.536e-17 s^3 + 4.035e-09 s^2
```

B.b Closed-Loop Response of the PLL

The closed loop (phase-transfer function) is given by: $H(s)=\frac{K_{pd}K_{lp}K_{osc}H_{lp}(s)/s}{1+L(s)}=\frac{N\,x\,L(s)}{1+L(s)}$

The closed loop response, both the time-domain step response and the PLL phase transfer function are plotted below respectively.

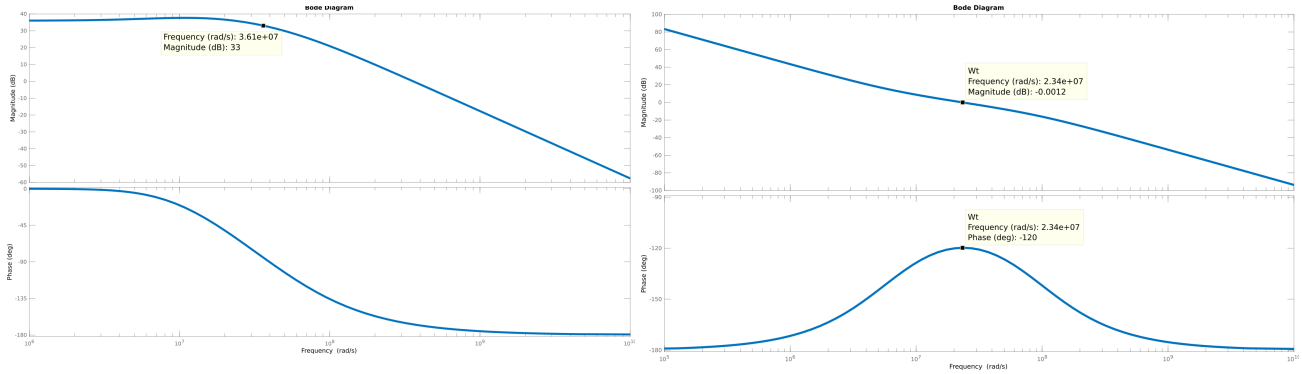




C. The effect of varying the N divider ratio in order to provide for a programmable frequency is as follows:

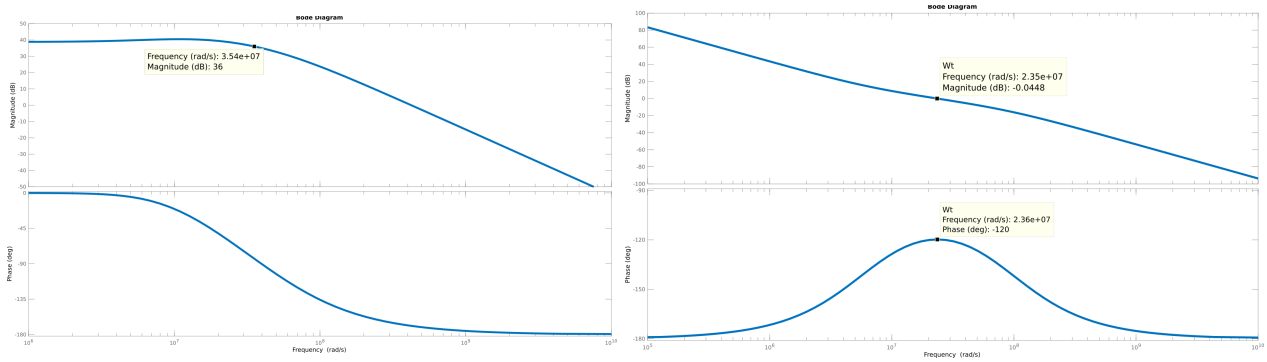
For 5.04GHz: $N=5.04\,GHz/80\,MHz=63$ **N = 63**

The decrease in divider ratio leads to an increase in closed-loop bandwidth whereas the PM remains similar as before (no noticeable difference). See both plots below



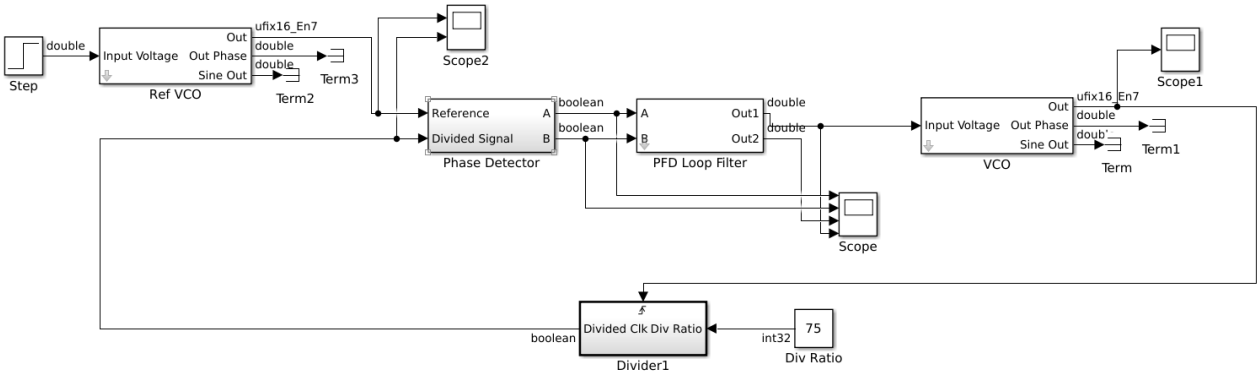
For 6.96GHz: $N = 6.96\,GHz / 80\,MHz = 87$ **N = 87**

The decrease in divider ratio leads to an decrease in closed-loop bandwidth whereas the PM remains similar as before (no noticeable difference). See both plots below



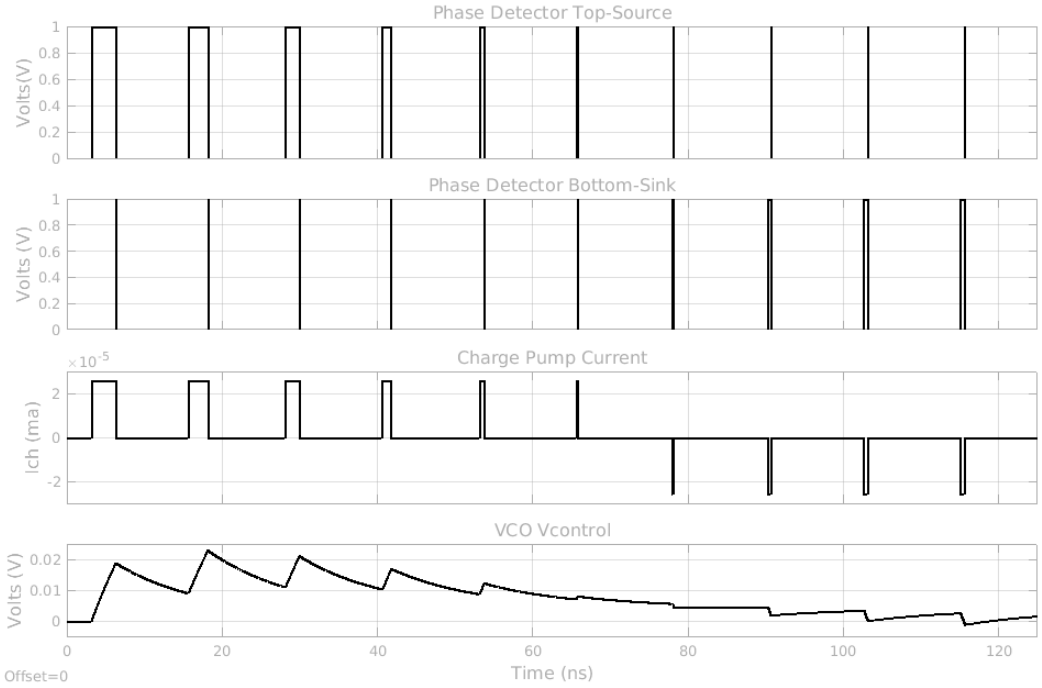
D. PLL Simulink Model (Based on our PLL Design Parameters)

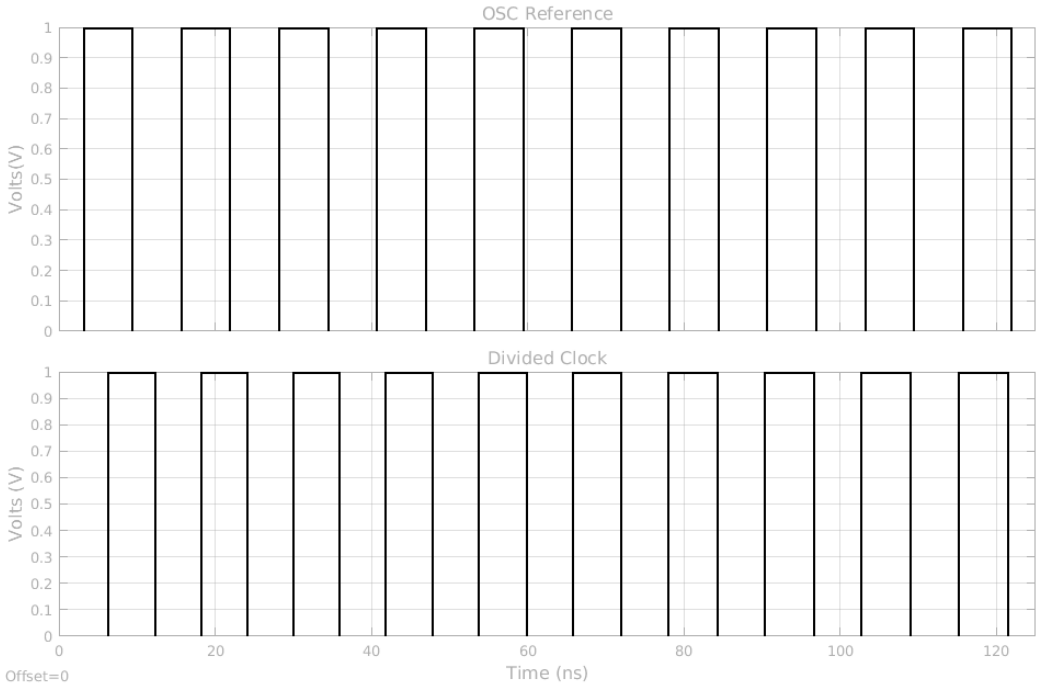
Using the parameters for the PLL designed above and the provided simulink PLL examples, the following is a block diagram for our PLL

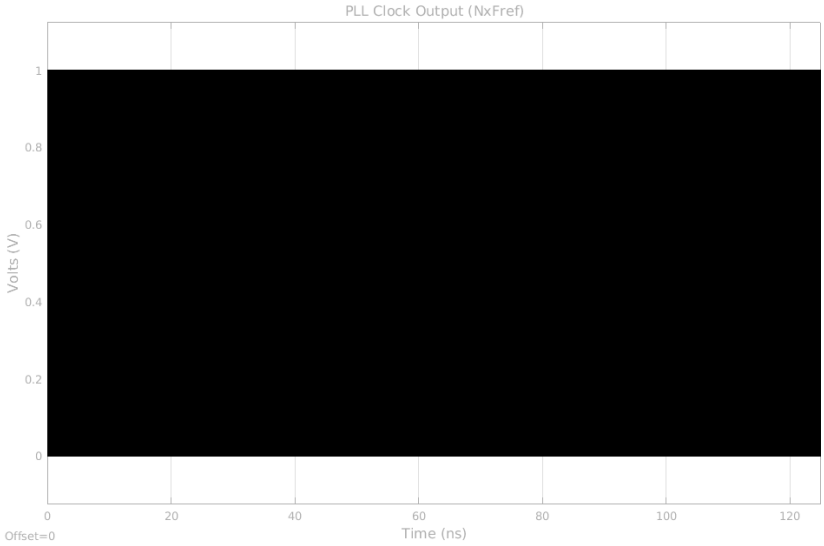


E. The following are plots taken at the output of the phase detector, the charge pump current waveform, the VCO control voltage, the PLL output clock, and N divider output and the input reference clock all plotted with the same time axis for ease of inspection.

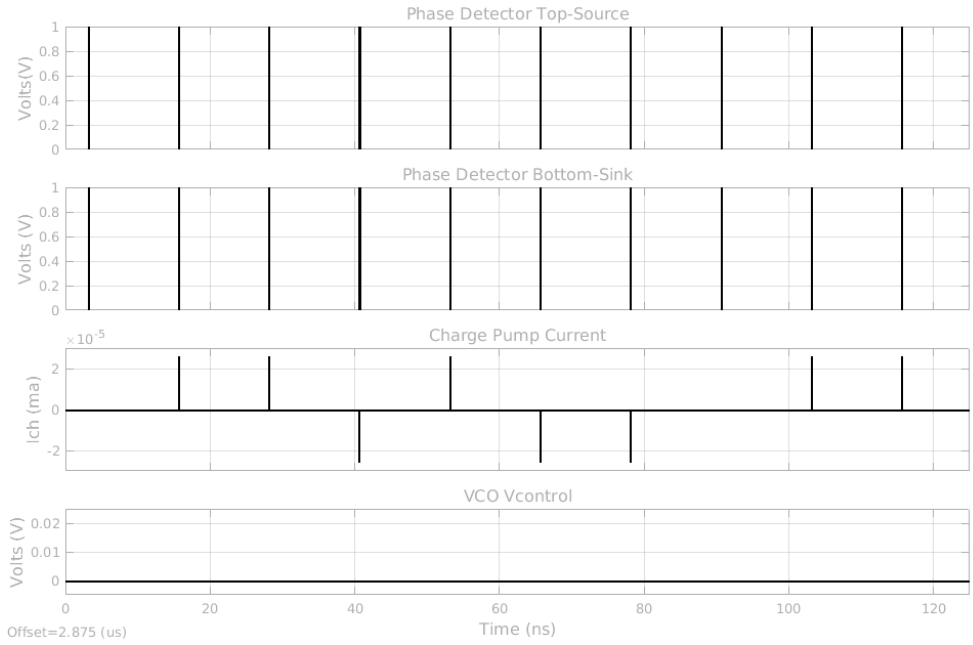
The PLL not yet in lock

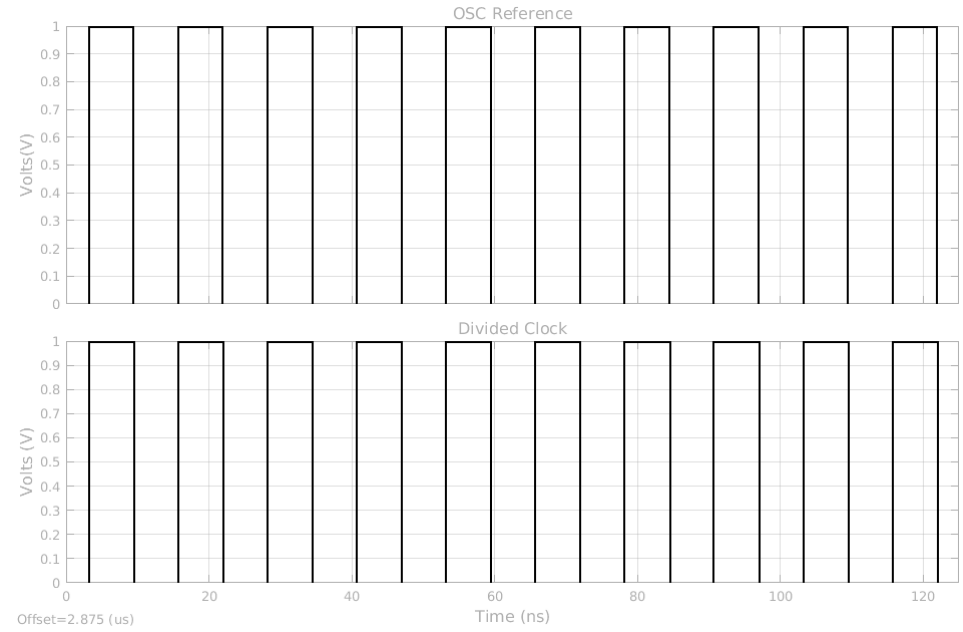


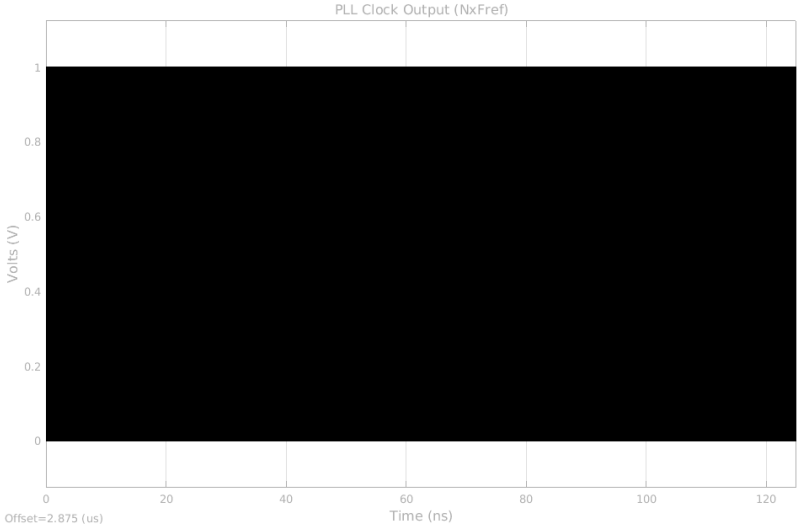




The PLL in lock





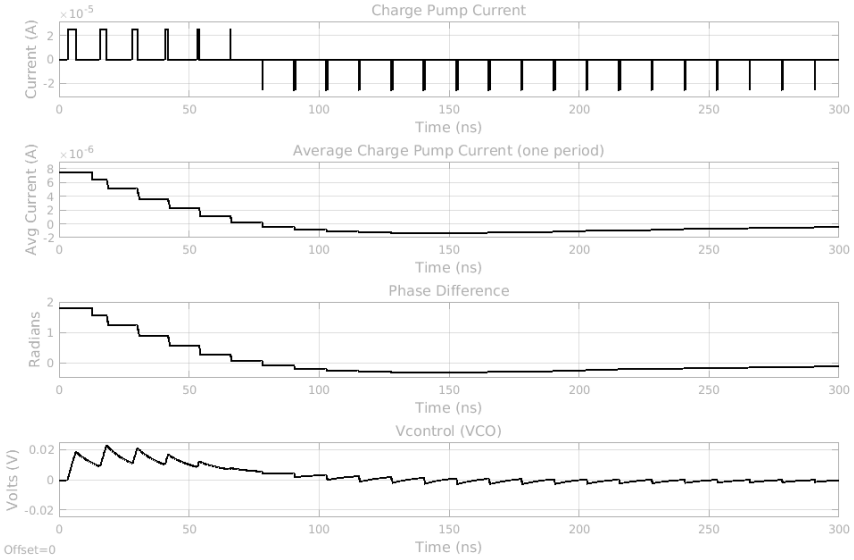


F. For this question we have to provide plots of Vcntl vs time and phase difference vs time.

- During initial locking of the PLL, and
- After locking, and upon a change in reference frequency by 0.1%

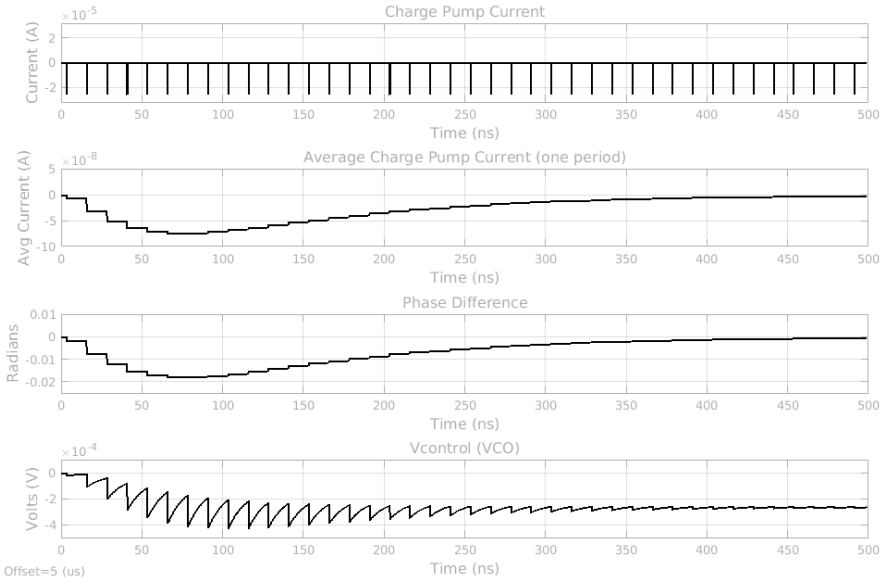
During initial locking of the PLL

For this question we calculate Vcntl vs. time as before, for the phase difference we can calculate from our phase detector transfer function $K_{pd} = I_{ch}/2\pi = 25.95\mu A/2\pi = 4.1301\mu A/rad$ Here then we can calculate our phase difference as: $\phi_d = I_{avg}/K_{pd}$ where Iavg is the current averaged per period. To calculate this average we are using the "mean" simulink block (over one period), and the division we implement as a gain multiplier block. The following are our plots:



Upon change in reference frequency by 0.1% (new fref = 79.92MHz)

we implement this change in frequency with the step block by initially starting at a set value of 1, and then stepping down to 0.999 (keeping the reference Kvco constant at 2*pi*80MHz)



The y axes have been scaled to visualize the waveforms (smaller than during initial locking), also note Vcontrol will settle to a small negative value since VCO center freq is set at 6GHz nominally.

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