Part 1

For part I, we are asked to design a fully-differential closed-loop programable gain Opamp with the following specifications:

Gain (closed-loop measurement):

- Programmable: 4, 8, 12, or 16 V/V

-3db Bandwidth (closed-loop measurement):

Phase Margin (open-loop measurement)

- Greater or equal to 70 degrees

Noise input referred (integrated input referred noise over bandwidth)

- Less or equal to 100uVrms at high-gain setting

Biasing Circuit

- All bias circuitry on-chip, with only 1 off-chip precision resistor available.

Topology Selection

Initially starting from the single-ended opamp design, the decision was whether the use of a single-stage, a single-stage approximation or 2-stage opamp. More stages normally are advantageous to enhance the gain of an amplifier (for example the standard diff pair + common source topology), however with more stages also comes more parasitics and hence reduced bandwidth, or said otherwise it becomes increasingly difficult to stabilize the opamp to achieve a larger bandwidth (recall the largest bandwidth that can be achieved is that of the ft of a single stage transistor amplifier)

Therefore in principle, for a single-stage:

- Gain is limited: by the gm x rout of one transistor (assuming single transistor amplifier)
- Bandwidth is maximum: only limited by ft of single-transistor and op. condition biasing
- Compensation is simpler: output compensation (dominant pole) is often sufficient

Special topologies (e.g. folded cascode opamp, or current-mirror opamp or telescopic cascode opamp) albeit by their own nature consisting of more than one pole can be effectively designed as single-pole approximations, this topologies can alleviate the gain limitations of a purely single-stage amplifier while still being approximated and designed as single dominant pole systems.

For 2-stage opamps:

- Gain is large: consisting of the gain of each stage

- Bandwidth is reduced: limited by the poles introduced by each stage (which now need to be compensated for)
- Compensation is more difficult: you need a compensation strategy for the additional node-poles introduced in the circuit

In the case of opamps which are meant to be used in a closed-loop configuration we require a high enough open-loop gain. (sometimes greater that what a single transistor can provide you)

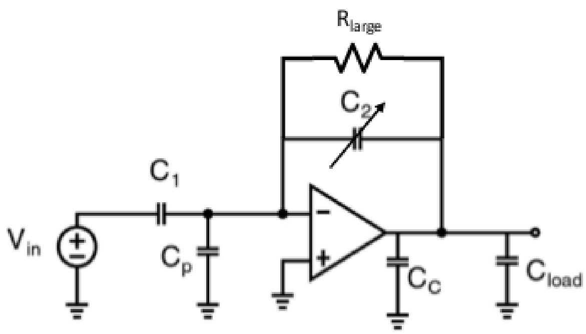
I.e normally if you can “get away” with a single-stage, i.e. if you can meet your desired gain for your application with a single stage, this is often the way to go.

Single-stage amplifiers (e.g. for RF or high-speed amplifiers applications) have large bandwidth but gain may be insufficient for opamp applications. Single-stage “approximated” amplifiers have enhanced gain and sufficient bandwidth (often a good tradeoff for analog opamps): often a good compromise for analog opamps. Multi-stage amplifiers can yield larger gain but are difficult to compensate to attain the same bandwidth

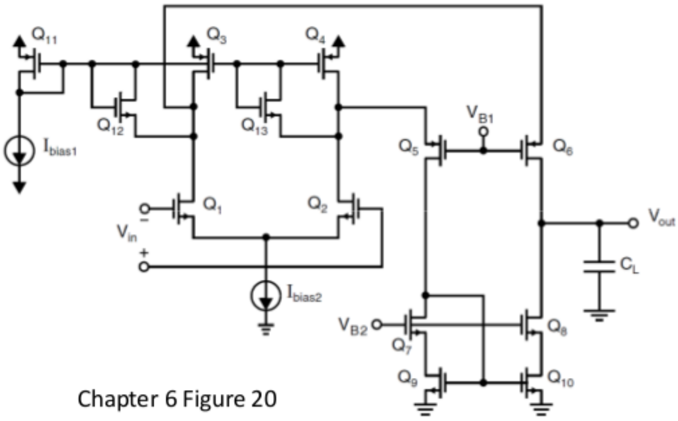
In our case given a 3db bandwidth of 50MHz in the closed loop and a max gain of 16, we need to attain a intrinsic opamp bandwidth larger than approximately around >800MHz (precise calculation below) with sufficient intrinsic gain around 70dB (precise calculation below).

We opted to use a single-stage approximation design – a folded-cascode opamp – which should support a bandwidth larger than our requirement, an easier compensation procedure to attain our phase margin, noise primarily dependent on the input capacitor (which we have control over) and a maximum gain in the vicinity of around 70dB with the option of gain boosting if necessary to meet our gain error (this assumption was accurate as will be seen later, to maintain close loop error below 0.25% we required the use of gain boosting to meet the gain error spec).

Following the lecture material, there are some good example references to aid in understanding the design for programmable gain feedback amplifiers. In our case, if we limit our feedback to a capacitive network it is possible to employ the simpler single-stage “dominant pole” amplifiers, and the book reference (section 6.6) elaborates on calculating the effective load capacitance we need to account for in our bandwidth calculations for this kind of opamps (explained below). In addition, and perhaps most importantly we have a reference design procedure outlined in the book, and a reference design which we explored and gained insight for in assignment 1. The general topology for the closed-loop amplifier we decided to design for was:



With, the general topology for the single-ended folded cascode opamp as:



Chapter 6 Figure 20

Design Procedure (for folded cascode Opamp)

Note (what didn't work): for future reference

(1) Initially a lot of time was spent unnecessarily working backwards from the previous assignment 1 design to aim to increase current (while tabulating and measuring the devices operating region to maintain them in saturation) to increase gm of the input pair, this was very time consuming and lead to suboptimal results that ultimately we had little intuition for.

(2) After calculating our input capacitor given our noise spec, designing for said large capacitive load (and not the effective load) while meeting our bandwidth lead to unreasonably high gm values (order of gm around 13mS needed for the input par) which lead to unpractical current consumption values (on the order of 1mA for the tail current).

(3) After mis-calculating gm_in above and the necessary gain for our error spec, aiming to calculate the necessary output resistance and hence the gm and gds of transistors from first principles, to attain such gain spec – an unpractical experience.

After a lot of effort spent: <u>the following is the design procedure that we ultimately followed to arrive at our final results.</u>

1. NMOS and PMOS Characterization test-benches

Initially to get an idea for the performance we could get from our devices, we built two standard test-benches to find the (1) gm/Id per W to find our nominal device size, then (2) gm/Id curve to find the current necessary to bias our devices to attain the necessary gm spec (to be calculated later on).

We often went back to our characterization testbenches to size and bias transistors to achieve the necessary operating point.

2. Calculate C1 given the noise spec

Given our maximum input referred noise: $V_{\text{in,ir}} = 100uVrms$ and our equation for input referred noise $V^2_{\text{in,rms}} \simeq \frac{4\pi K T \gamma}{C_1}$ therefore $C_1 = \frac{4\pi K T \gamma}{V^2_{\text{in,rms}}}$ which we calculated to be

$C_1 = \frac{4\pi 1.38\, x\, 10^{-23}\, jK^{-1}\, x\, 298.15\, x\, 0.521}{100\, uV^2} = 2.694\, pF$ Therefore we chose to use a value of **C1= 2.7pF**

Here our value of lambda was the average from that obtained for all transistors from spice simulations. (alternatively we could have used 2/3)

3. Calculate C2 given gain spec

From our maximum and minimum gain spec we can calculate the values of **C2_min=168.75fF and C2_max=675fF.**

4. From the bandwidth and capacitive network calculate necessary gm of input pair

(section 6.6 from reference textbook, and general topology diagram above)

The canonical expression for the intrinsic unity gain frequency of the amplifier: $w_{ta} = gm \frac{1}{C_{effective}}$

Where Ceffective is important for the design of the folded cascode amplifiers: the effective load the amplifier needs to drive. $C_{effective} = Cc + C_{load} + \frac{C_2(C_1 + C_p)}{C_1 + C_p + C_2}$

In our case, as our amplifier is operated without a subsequent load and we aim to use the effective capacitance itself to achieve dominant pole compensation (without the use of additional Cc), we can assume **Cc = 0, Cload = 0, C2_max=675fF, C2_min=168.75fF, C1 = 2.7pF** and we can calculate our parasitic capacitance as half of the Cgs of our input pair at max dimensions (W=180um) i.e. Cp=Cgs/2 where $C_{gs} = (\frac{2}{3}) W_{M1} \, x \, L_{M1} \, x \, C_{ox} = \frac{2}{3} \, x \, 180 \, x \, 0.4 \, x \, 8.5 fF/um = 408 fF$ and hence **Cp=204fF** Therefore we can calculate Ceffective for two cases where C2 is max and min.

$$C_{\text{effective\_max}} = \frac{C_2(C_1 + C_p)}{C_1 + C_p + C_2} = \frac{675 fF \, x \, (2.7 \, pF + 204 fF)}{2.7 \, pF + 204 fF + 675 fF} = 547.7 \, fF$$ and similarly $C_{\text{effective\_min}} = 159.5 \, fF$

At this point we need to calculate the necessary intrinsic Ft of the opamp, given:

$W_{ta} = W_t / \beta$ Here it is important to remember that for the open-loop response (including the feedback network), wt is equal to the closed loop -3db bandwidth of the closed-loop amplifier i.e.

$W_{\text{t (open-loop)}} = W_{\text{-3db (closed-loop)}}$ in our case then $f_{\text{-3db (closed-loop)}} = 50 \, MHz = f_{\text{t (open-loop)}}$

Additionally the feedback factor of the network can be calculated as:

$$\beta_{\max} = \frac{C_2}{C_1 + C_p + C_2} = 0.189$$ and $\beta_{\min} = 0.055$

Now we can calculate the intrinsic unity gain for the opamp as:

$W_{\text{ta\_max}} = W_t / \beta = \frac{2\pi 50 MHz}{\beta_{min}}$ giving $F_{\text{ta\_max}} = 909.09 \, MHz \sim 910 \, MHz$ and similarly $F_{\text{ta\_min}} = 265.1 \, MHz \sim 265 \, MHz$ therefore we should design for Fta in the vicinity of 900MHz to meet our bandwidth requirements.

Hence, at this point we can calculate the necessary gm for our input pair to meet our bandwidth as:

$$gm_1 = w_{\text{ta\_max}} \, x \, C_{\text{effective\_max}} \simeq 3.133 \, mS$$

5. Calculate Id and sizing needed for input pair devices

Now that we know the necessary transconductance of the input pair, we want to choose the largest practical device (180um largest, from book reference) to yield the greatest gm and lowest Veff: *this transistor is to be operated at the verge of sub-thresshold to attain a large transconductor efficiency (gm/Id).*

We know the bias current for each input transistor must necessarily be larger than that achieved under sub-threshold operation (max limit for gm/id trans-conductor efficiency), in our case:

$$I_{\text{d\_min}} = \frac{gm_1 \, x \, n \, KT}{q} = 128.7 \, uA$$

Now we went on to our NMOS characterization testbench to obtain the necessary Id current given gm1=3.133mS, W=180um and Veff=0. Our results show that we need to bias at **Id1,2=151.7uA ~ 150uA.**

6. Calculate bias currents based on input pair current requirements

Our input pair requires a total bias current of **Ibias2~300uA**. Furthermore we are recommended from the book to allocate the total current in a 4:1 ratio as: $I_{\text{in\_pair}} = 4 \, x \, I_{\text{casc}}$ In our case this translates to **Icasc = 75uA** (**I5,6=37.5uA),** leading to a total current of **375uA (I3,4=187.5uA).**

Setting the bias reference current to 1/10 that of I3,4 then yields **Ibias1=18.75uA~20uA.**

7. Calculate transistor sizes based on current estimates for each device

(enforce Veff~0.24 and saturation operating region)

Knowing the drain current required for each device, the effective overdrive voltage, the operating saturation region and the minimum length (Lmin=400nm) for each device, we can calculate approximate transistor sizes as:

M1,2: 180um (largest from book reference)

M3,4: $W_{3,4} = \frac{2 \, x \, I_{d3,4}}{\mu_p C_{ox} V_{eff}^2} \, x \, L_{min} = 37.64 \, \mu m \sim 40 \, \mu m$ similarly for the M5 and M6 PMOs devices,

M5,6: $W_{5,6} = 7.44 \, \mu m \sim 8 \, \mu m$

M7,8=M9,10: $W_{7,8} = \frac{2 \, x \, I_{d5,6}}{\mu_n C_{ox} V_{eff}^2} \, x \, L_{min} = 1.95 \, \mu m \sim 2 \, \mu m$

M11: W11=W3,4 / 10 = 3.76um ~ 4um (recall Ibias1 is ¼ of I3,4)

M12,13: these are the slew-rate helper clamp transistors (chosen to be minimum dimensions).

8. Determine bias voltages (vb1 and vb2)

(assuming Veff~0.24)

Vb2: Here M9 and M10 are part of our NMOS wide swing current mirror where it is desirable that they have the lowest Vds but without going into triode. From section 6.31 and assuming Veff=0.24

$V_{\text{gs 9,10}} = V_{tn} + V_{eff} \sim 450 \, mV + 240 \, mV \sim 690 \, mV$ therefore since we bias right before entering triode $V_{\text{ds 3,4}} = V_{\text{ds\_sat 3,4}} = 240 \, mV$ Therefore we can calculate Vb2 as:

$V_{\text{b2}} = V_{\text{ds 3,4}} + V_{\text{gs 7,8}} = 240 \, mV + (450 \, mV + 240 \, mV) \geq 930 \, mV$ We choose our bias source Vb2 to be 1.05 (same as that for assignment 1)

Vb1: M5 and M6 are a symmetrical PMOS cascode (to M7 and M8) which we can take to have a PMOS cascode voltage of $V_{M\,5,6}=1.8-Vb2=1.8-1.05=750\,mV$

9. Calculate required intrinsic amplifier gain given closed loop gain error

The opamp closed loop error can be given by:

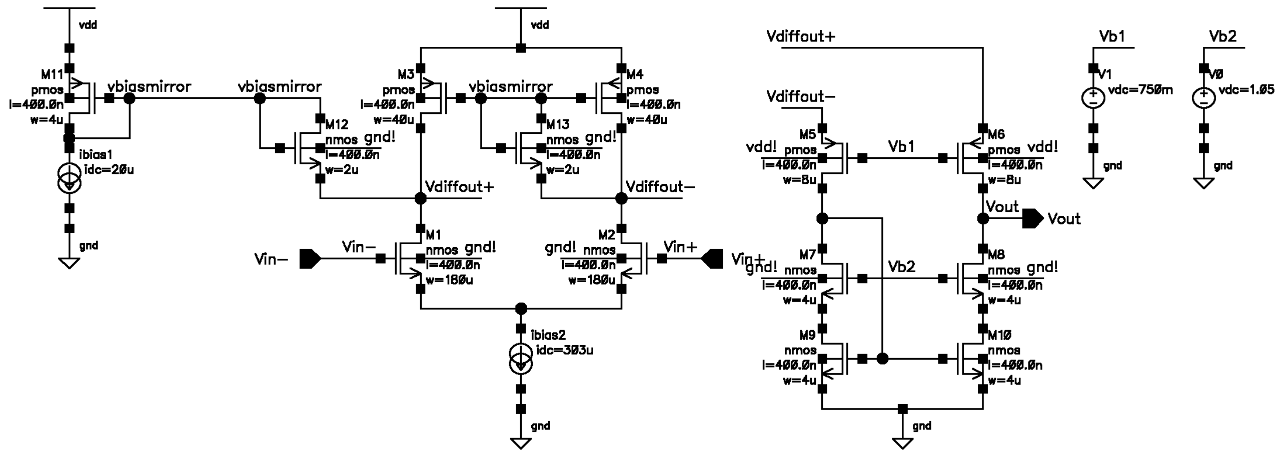
$V_{b2}=V_{ds\,3,4}+V_{gs\,7,8}=240\,mV+(450\,mV+240\,mV)\geq 930\,mV$ N: is represent the *additional* open-loop intrinsic amplifier gain needed in order to achieve the gain error spec, therefore in our case (0.25% error):

$$N=\frac{1}{\delta}-1=\frac{1}{0.0025}-1=399\,V/V=52.019\,dB$$

And our maximum closed-loop gain at 16V/V is 24.082dB, therefore our minimum open loop gain we need to have to meet the error spec: $A_{a\_db}=N_{db}+A_{cl\_max\_db}=76.102\,dB$

Unfortunately the folded cascode topology can reach up to approximately 70dB of gain, thus we will require a way of enhancing our gain through the use of gain boosting.

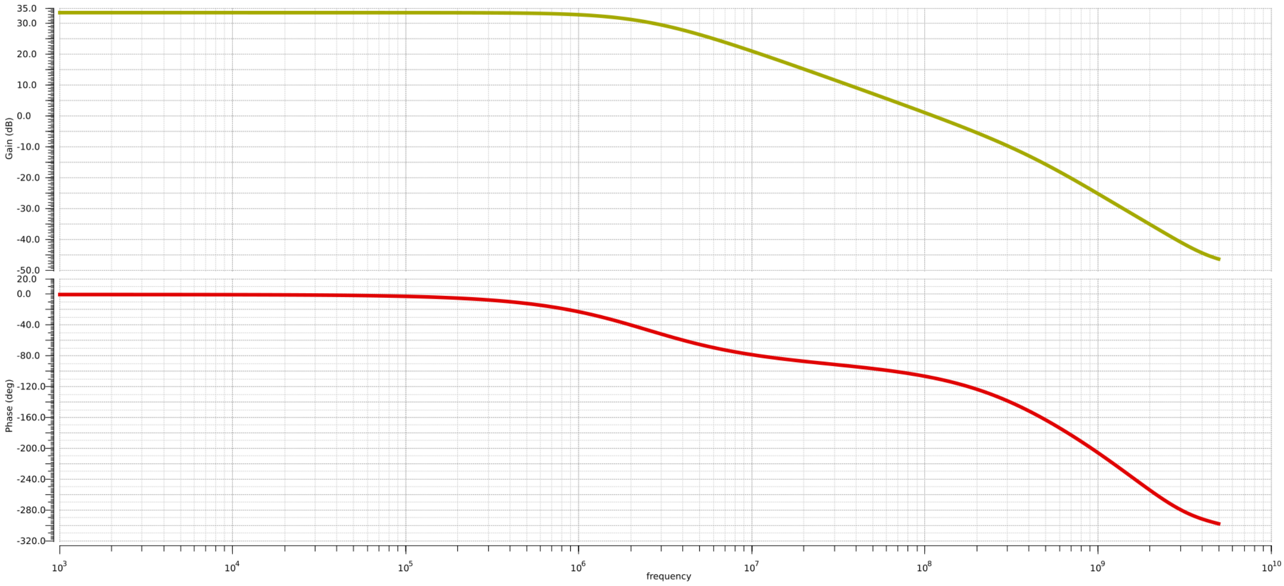
The final single ended amplifier design with sizes can be seen below:

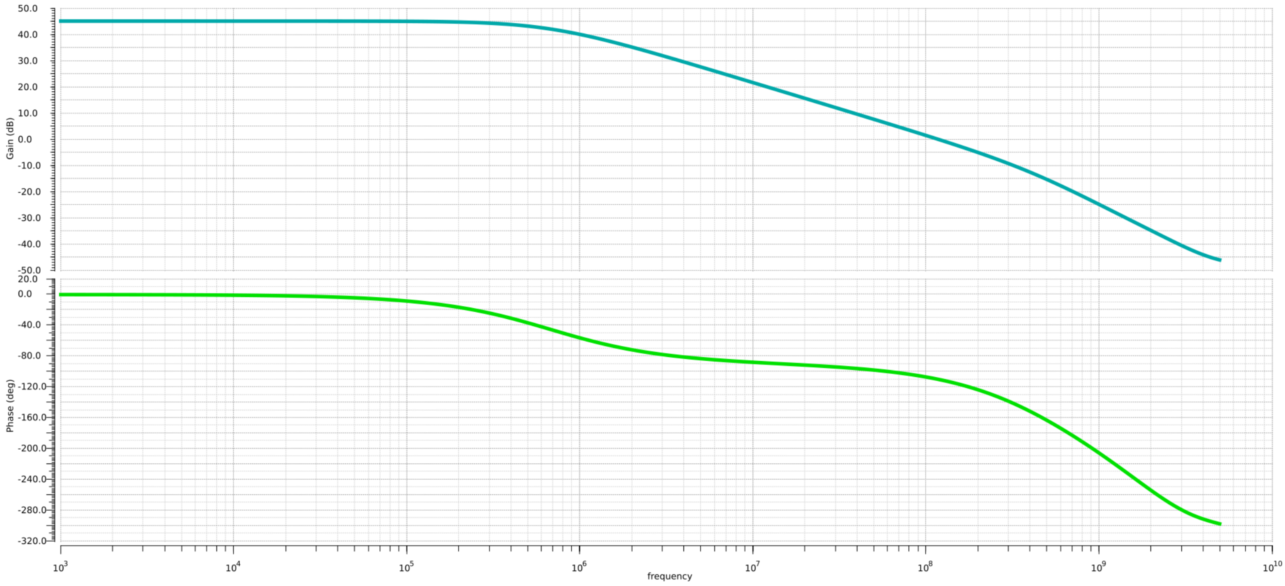


Note the M7-10 transistor sizes were increased to 4u, as this has a slight improvement in performance.

Single-ended Open Loop Response

The following is the open loop response of the single-ended amplifier at maximum gain setting and minimum gain setting (open-loop dc gain $L = A_a x \beta$). Recall from our calculations the open loop unity gain frequency should be greater than 50MHz (Ft>=50MHz), and our phase margin greater than 70 degrees.





Results at max gain setting and min gain setting

Ft cross	114M
Phase Margin	71.42

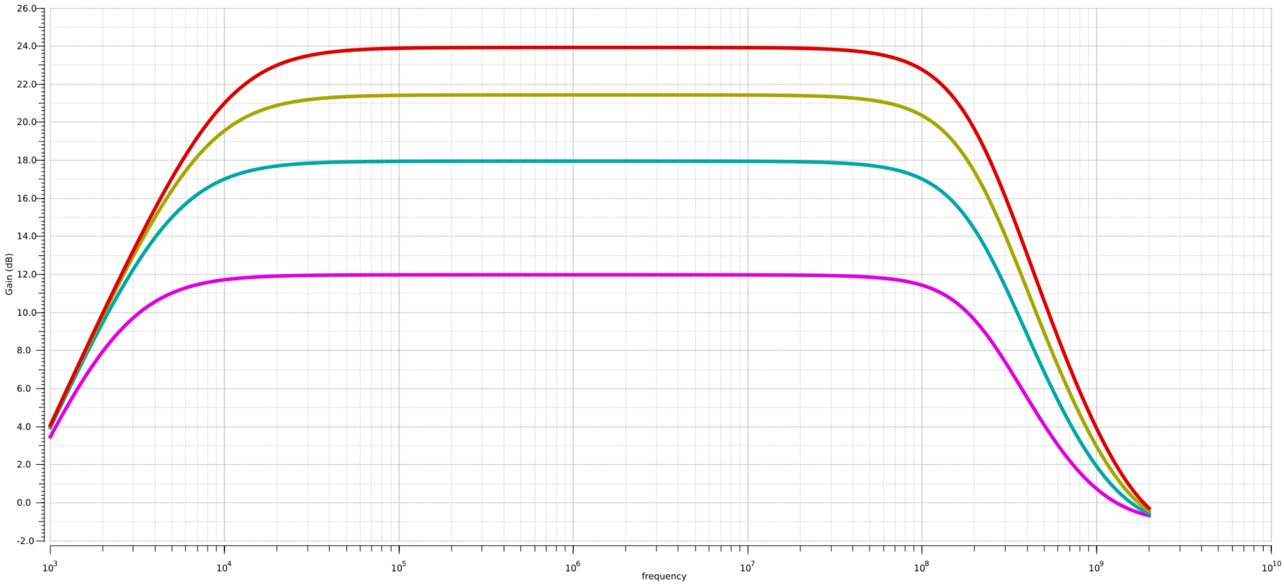
Ft cross	118.7M
Phase Margin	69.79

Our results indicate a open-loop unity gain frequency much larger than our required 50MHz and a phase margin of around 70 degrees.

Single-ended Closed Loop Response

Now we go on to the closed-loop amplifier testbench (same as assignment 1) and verify the performance of the Opamp.

The following is the closed loop response at all of the gain settings. A resistor Rlarge=95MΩ was used to help with convergence and to set the 10KHz lower bandwidth.

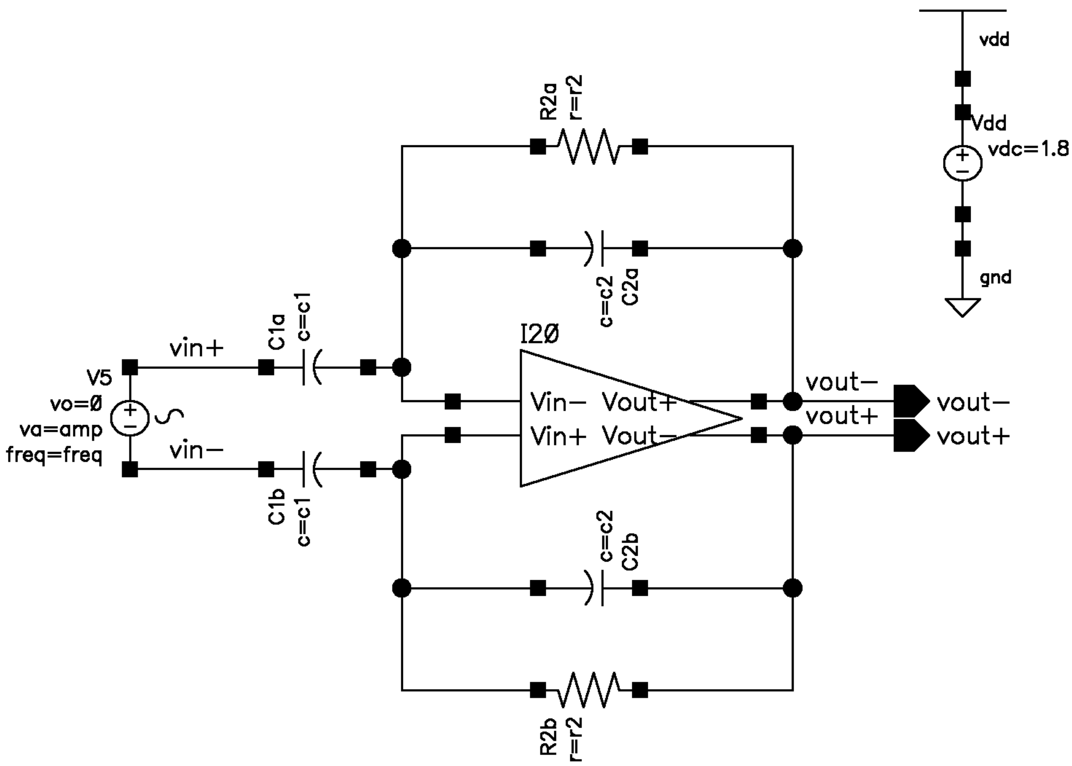


Note for the worst case (at max 24dB gain) the -3db bandwidth measured at 21dB is greater than 100MHz and larger than the necessary 50MHz – Meeting our bandwidth spec for the single ended opamp. The gain spec is very close but indeed if one zooms in, it is possible to see the gain error.

Fully Differential Folded Cascode Opamp

(see results at the bottom of this section)

Having our single-ended amplifier, now we moved incrementally towards making our opamp fully differential using our differential amplifier closed-loop response testbench (below), the following are the steps we followed sequentially:



1. Initially we started from our single-ended design by disconnecting the gate for M9 and M10 and connecting it directly to be driven by an ideal current mirror NMOS bias voltage (with same dimensions), this means we provided the bias voltages for the bottom NMOS and cascode NMOS and upper PMOS and cascode PMOS with ideal sources (or mirrored sources).

2. Next we checked for the correct operating point for each transistor, otherwise updating the bias sources accordingly to have all transistors in saturation.

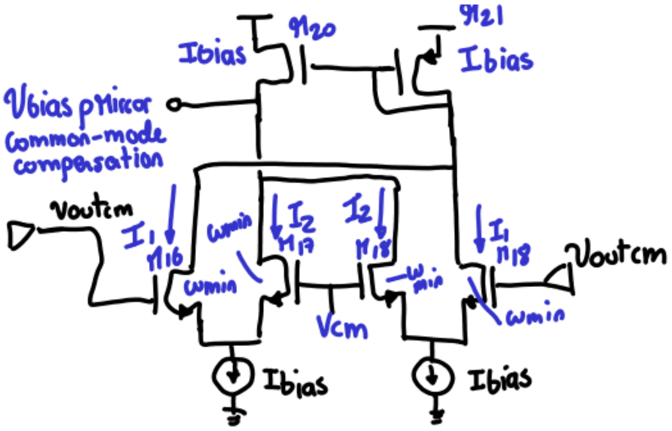
3. Next we applied a very small signal and measured the transient output response at time=t0, before common-mode slow drift to the supply rails took place.

- We verified the desired time-domain operation of the amplifier

4. Next we did an AC analysis identical to that for our single-ended closed loop amplifier to verify equal performance but now differential input and output.

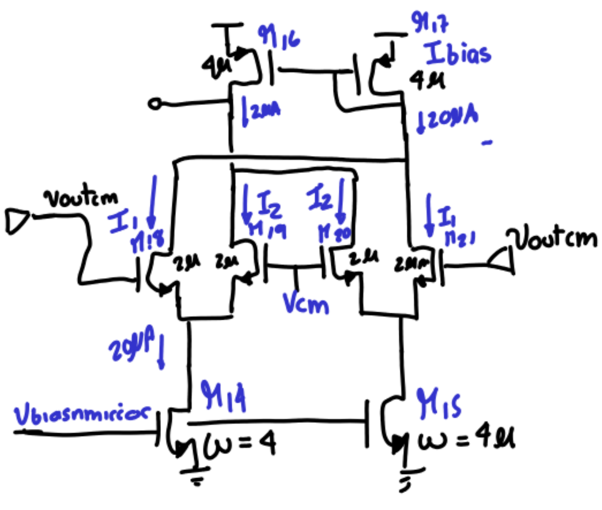
The initial performance (without CMFB and ideal sources) of the differential design was thus tested.

5. At this point we proceeded to the design of the CMFB circuit, we decided to use a CMFB circuit presented in **reference [1]** which outlines the principles of operation and was intuitive to understand.



Intuitively we see that if Voutcm is equal to our desired setpoint of Vcm then we have no common-mode error and the branch currents divide equally, and I bias is mirrored (and scaled) to our upper PMOS devices in our Opamp.

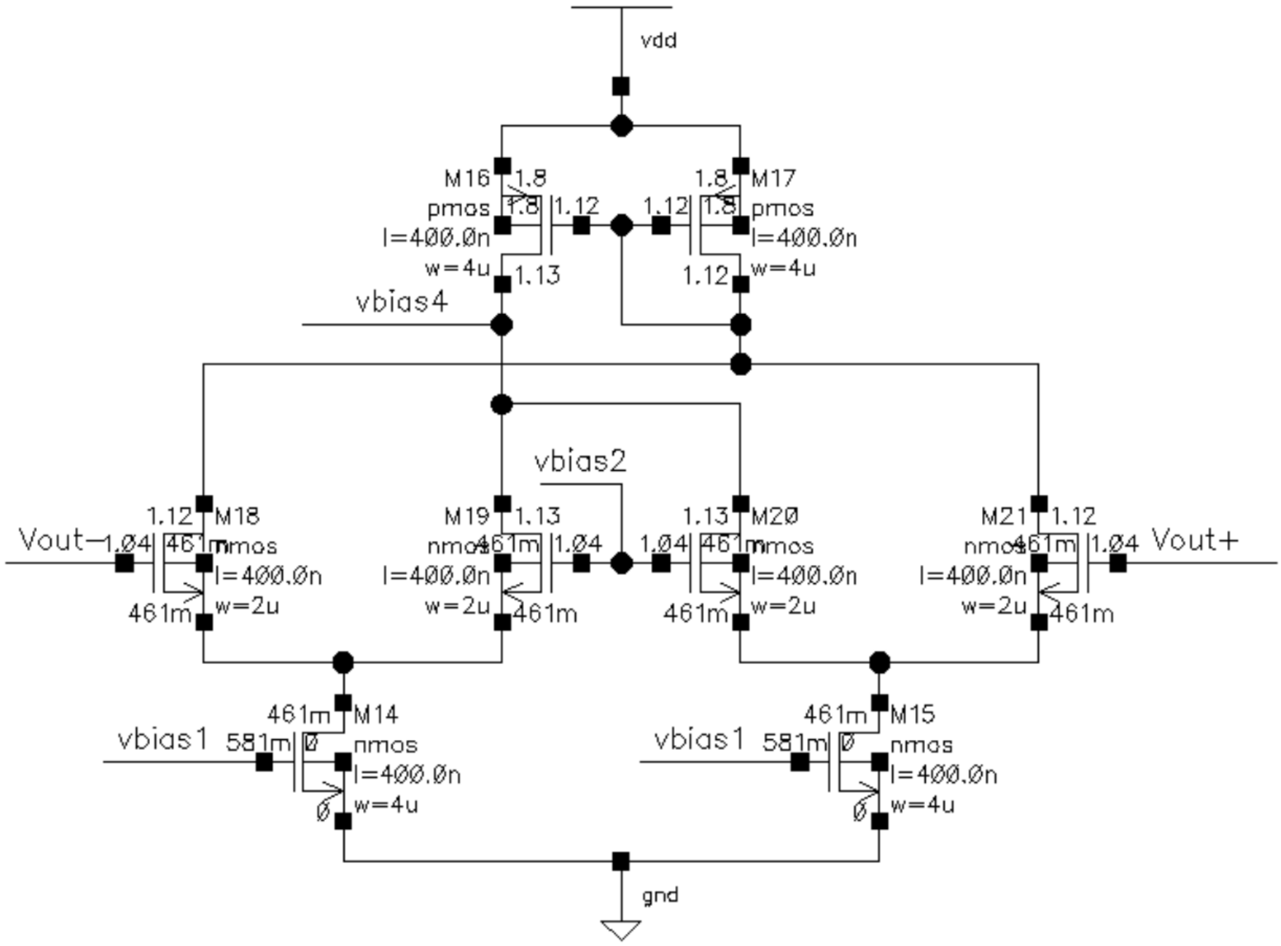
If however Voutcm increases above the desired Vcm current I1 increases and correspondingly current I2 decreases. If Voutcm decreases above Vcm current I2 increases and I1 decreases. Hence we have $\Delta I \propto V_{cm\_error}$ where Vcm_error is: our sensed Voutcm minus our desired Vcm setpoint. This Ibias plus/minus ΔI is mirrored to our Opamp PMOS top mirror and introduces a negative feedback loop to reduce the common-mode error until I1=I2.



We size our mirror devices to have the same 4um dimensions as our M11 reference transistor to carry the same 20uA of bias current.

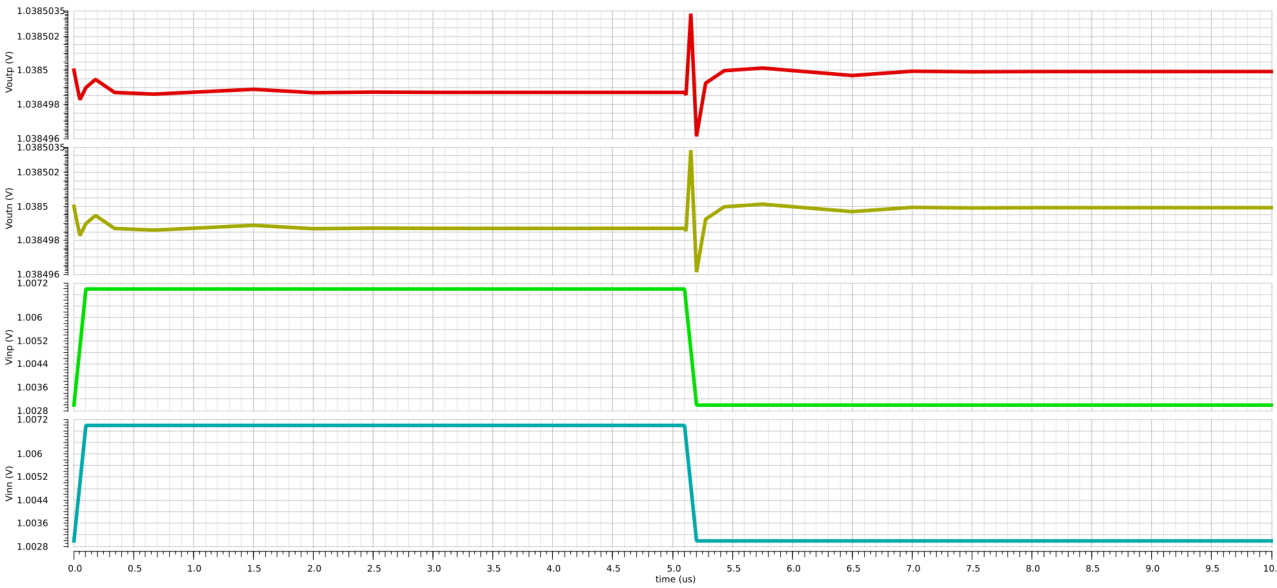
We size our differential pair devices with minimum dimensions to present a negligible load to the output and maintain the desired bandwidth spec.

The following is the CMFB circuit with sizes and annotated node voltages:



6. Next we define our Vcm voltage and test the operating point to make sure our CMFB circuit works at dc.

7. We then test our common-mode circuit by applying a common-mode step at the input and inspecting the settling time to the common-mode setpoint at the output.



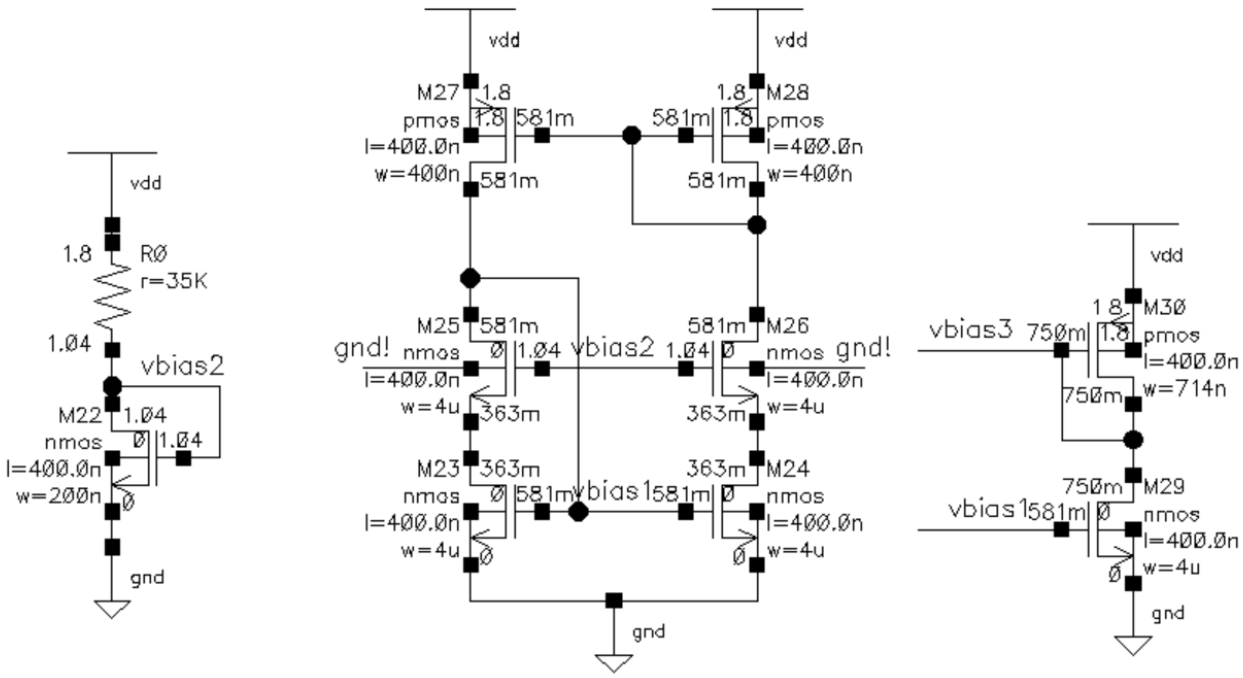
(note here a small common-mode 5mV step was applied with reasonable 100nS rise/fall times)

8. We next moved to replace all ideal biasing sources and utilize only one off-chip resistor.

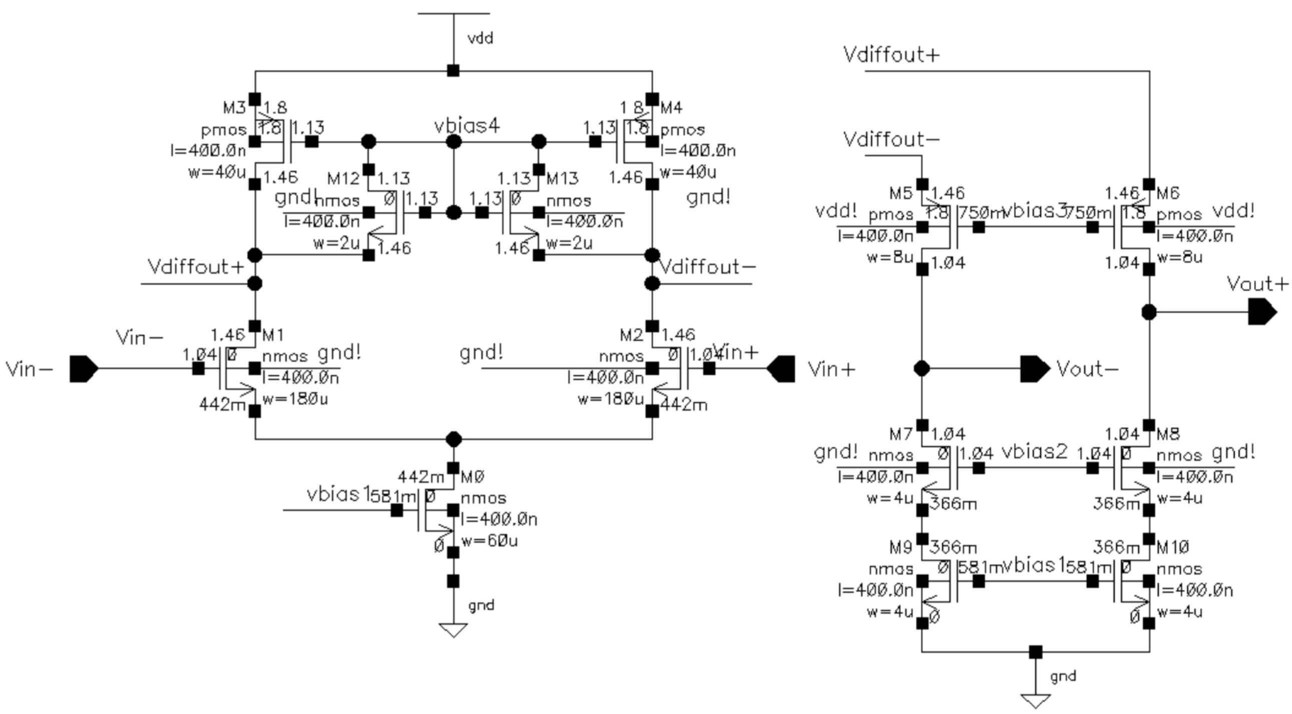
Our main need here was to generate the biasing required for: (1) The bottom NMOS current mirrors and tail current source (2) The NMOS cascode in the wide-swing current mirror (3) The biasing for the PMOS cascode.

Note the PMOS current mirror is driven by the CMFB circuit directly, and the common-mode voltage setpoint can be chosen from one of the generated bias voltages.

In our case we decided to use a wide swing current mirror for generating most of the bias references needed in the Opamp. The following is the biasing circuit, as well as the generated voltages to be used for the circuit.

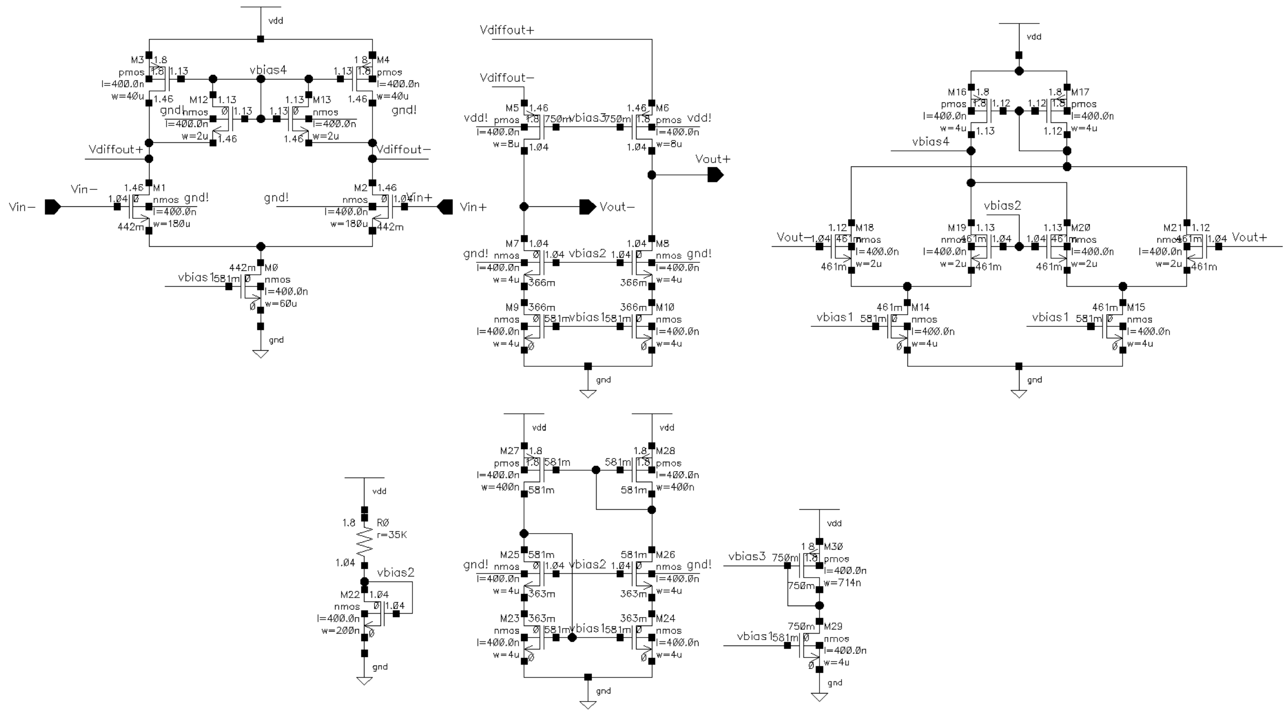


The following is the differential Opamp schematic with device sizes and annotated node voltages



The full schematic (without gain boosting) with device sizes and annotated node voltages:

(easier to see above)



Operating point for each of the transistors (slew rate clamp transistors 12,13 normally in cuttoff)

element	1:m0	1:m1	1:m2	1:m3	1:m4	1:m5	1:m6	1:m7	1:m8	1:m9	1:m10	1:m12
model	0:nmos	0:nmos	0:nmos	0:pmos	0:pmos	0:pmos	0:pmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Cutoff
id	2.797E-04	1.398E-04	1.398E-04	-1.585E-04	-1.585E-04	-1.861E-05	-1.861E-05	1.861E-05	1.861E-05	1.861E-05	1.861E-05	-5.208E-16
vgs	5.809E-01	5.970E-01	5.970E-01	-6.693E-01	-6.693E-01	-7.110E-01	-7.110E-01	6.726E-01	6.726E-01	5.809E-01	5.809E-01	-3.305E-01
vds	4.415E-01	1.019E+00	1.019E+00	-3.388E-01	-3.388E-01	-4.227E-01	-4.227E-01	6.729E-01	6.729E-01	3.656E-01	3.656E-01	-3.305E-01
vth	4.594E-01	5.819E-01	5.819E-01	-4.560E-01	-4.560E-01	-5.540E-01	-5.540E-01	5.620E-01	5.620E-01	4.594E-01	4.594E-01	7.291E-01
vdsat	1.062E-01	6.012E-02	6.012E-02	-1.862E-01	-1.862E-01	-1.512E-01	-1.512E-01	1.090E-01	1.090E-01	1.062E-01	1.062E-01	4.231E-02
vod	1.215E-01	1.512E-02	1.512E-02	-2.132E-01	-2.132E-01	-1.570E-01	-1.570E-01	1.105E-01	1.105E-01	1.215E-01	1.215E-01	-1.059E+00
gm	4.184E-03	3.159E-03	3.159E-03	1.355E-03	1.355E-03	2.043E-04	2.043E-04	2.858E-04	2.858E-04	2.786E-04	2.786E-04	1.592E-14

element	1:m13	1:m14	1:m15	1:m16	1:m17	1:m18	1:m19	1:m20	1:m21	1:m22	1:m23	1:m24
model	0:nmos	0:nmos	0:nmos	0:pmos	0:pmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos
region	Cutoff	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	-5.208E-16	1.897E-05	1.897E-05	-1.895E-05	-1.900E-05	9.498E-06	9.473E-06	9.473E-06	9.497E-06	2.177E-05	1.860E-05	1.860E-05
vgs	-3.305E-01	5.809E-01	5.809E-01	-6.817E-01	-6.817E-01	5.777E-01	5.773E-01	5.773E-01	5.777E-01	1.038E+00	5.809E-01	5.809E-01
vds	-3.305E-01	4.608E-01	4.608E-01	-6.693E-01	-6.817E-01	6.575E-01	6.699E-01	6.699E-01	6.575E-01	1.038E+00	3.632E-01	3.632E-01
vth	7.291E-01	4.587E-01	4.587E-01	-4.525E-01	-4.525E-01	4.566E-01	4.565E-01	4.565E-01	4.566E-01	4.396E-01	4.594E-01	4.594E-01
vdsat	4.231E-02	1.066E-01	1.066E-01	-1.943E-01	-1.943E-01	1.059E-01	1.058E-01	1.058E-01	1.059E-01	3.792E-01	1.062E-01	1.062E-01
vod	-1.059E+00	1.222E-01	1.222E-01	-2.292E-01	-2.292E-01	1.211E-01	1.209E-01	1.209E-01	1.211E-01	5.985E-01	1.215E-01	1.215E-01
gm	1.592E-14	2.828E-04	2.828E-04	1.499E-04	1.501E-04	1.422E-04	1.420E-04	1.420E-04	1.422E-04	6.249E-05	2.784E-04	2.784E-04

element	1:m25	1:m26	1:m27	1:m28	1:m29	1:m30
model	0:nmos	0:nmos	0:pmos	0:pmos	0:nmos	0:pmos
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	1.860E-05	1.860E-05	-1.860E-05	-1.860E-05	1.995E-05	-1.995E-05
vgs	6.750E-01	6.750E-01	-1.219E+00	-1.219E+00	5.809E-01	-1.049E+00
vds	2.177E-01	2.177E-01	-1.219E+00	-1.219E+00	7.503E-01	-1.049E+00
vth	5.615E-01	5.615E-01	-4.248E-01	-4.248E-01	4.565E-01	-4.383E-01
vdsat	1.109E-01	1.109E-01	-5.801E-01	-5.801E-01	1.080E-01	-4.562E-01
vod	1.135E-01	1.135E-01	-7.943E-01	-7.943E-01	1.244E-01	-6.115E-01
gm	2.801E-04	2.801E-04	4.230E-05	4.230E-05	2.931E-04	5.719E-05

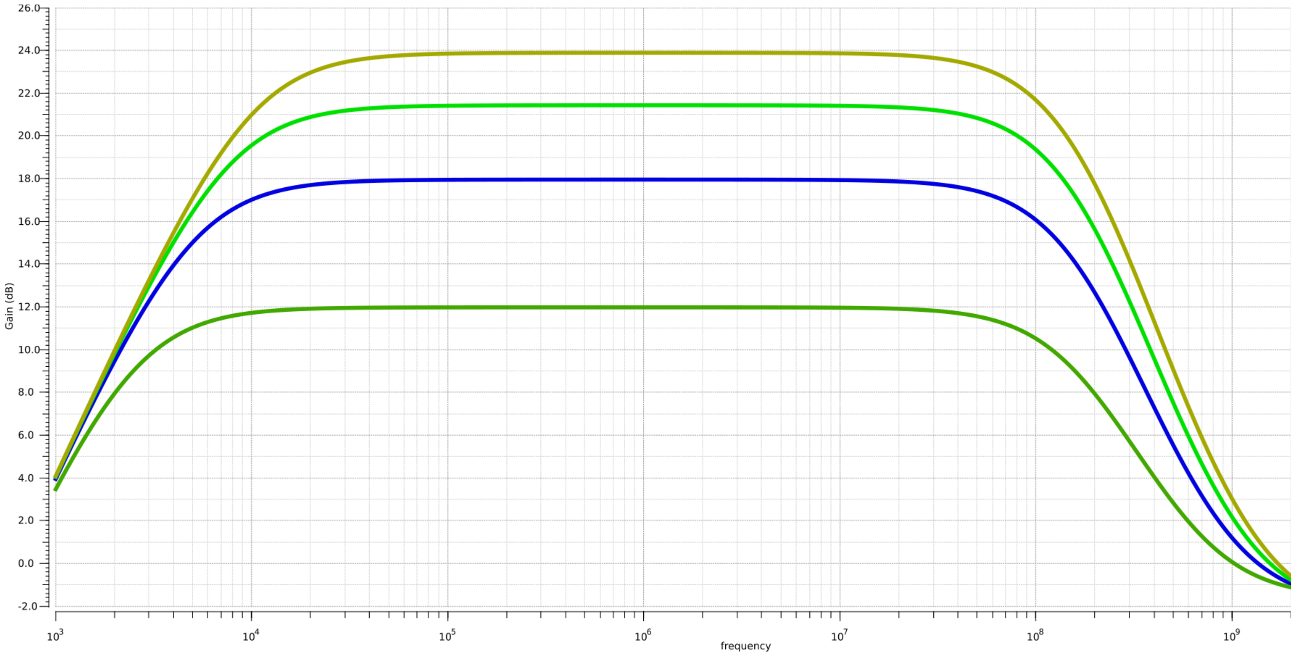
In the next section we present the results, measurement testbenches and finally the gain-boosting additions to meet the gain error specifications

Measurement Test-benches and Results

Fully-differential Closed Loop Response Results

(note the closed-loop test-bench was presented in the section above)

-3db bandwidth measurement and gain



Precise results (4x gain)

DC Gain	11.99
Loop Gain Magnitude	wave
-3DB Bandwidth	159.2M

Precise results (8x gain)

DC Gain	17.97
Loop Gain Magnitude	wave
-3DB Bandwidth	133.3M

Precise results (12x gain)

DC Gain	21.45
Loop Gain Magnitude	wave
-3DB Bandwidth	125.4M

Gain: 11.99 dB

-3dB BW: 159.2MHz

Gain: 17.97dB

-3dB BW: 133.3 MHz

Gain: 21.45 dB

-3dB BW: 125.4MHz

Precise results (16x gain)

DC Gain	23.94
Loop Gain Magnitude	wave
-3DB Bandwidth	120.5M

Note the gain figures are insufficient hence the use of gain boosting presented on next section

Gain: 23.94dB

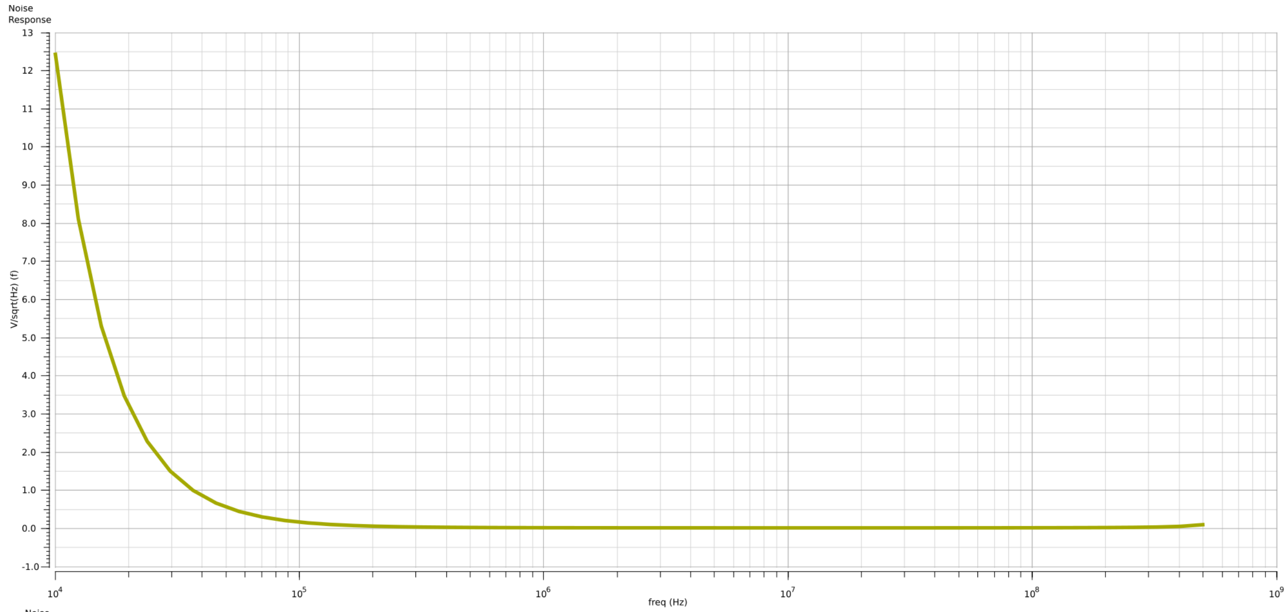
-3dB BW: 120.5M

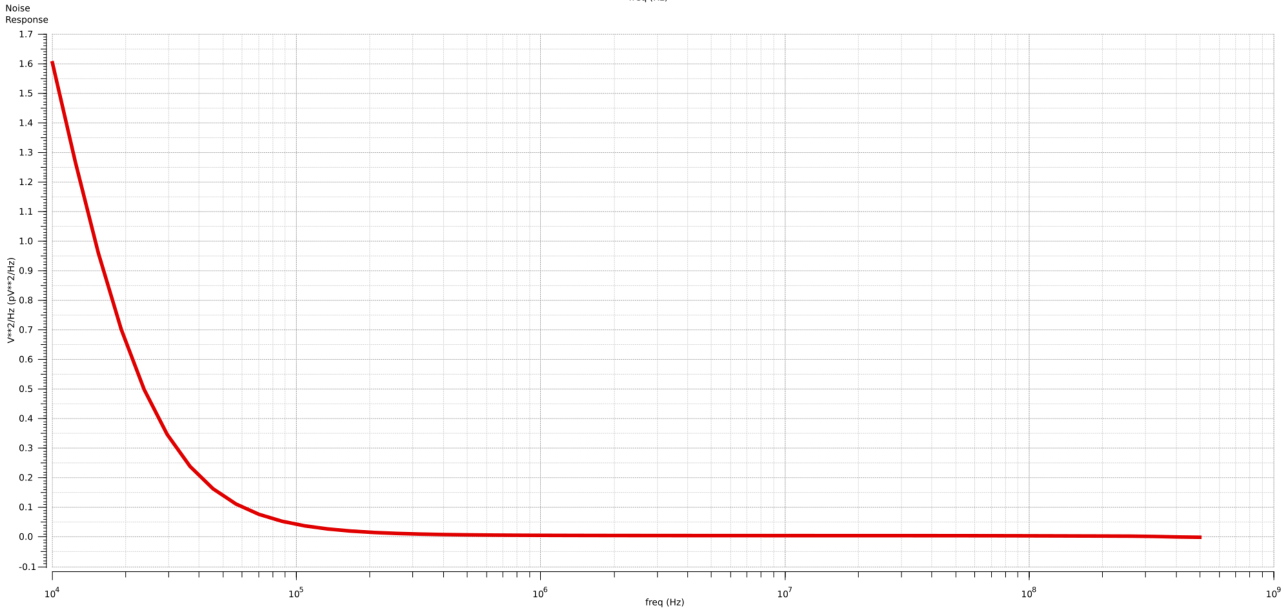
Note: The lower -3db Bandwidth was set precisely at 10KHz for the worst case (at 16x gain). For all other gains, the lower -3dB bandwidth is below 10KHz as required. (this result can be verified above).

Noise measurements

The input referred noise measurement was performed using the IRN – Simulation Setup presented from the lecture slides (58-62) over the frequency range of interest (10KHz – 500MHz) with the outputs taken differentially.

The input and output noise spectra are displayed below respectively (note the units are V/sqrt(Hz) and V^2/Hz respectively):





And finally the noise summary gives us our **Input Referred Noise** in uVrms integrated over our bandwidth. (**Vn,in,ir = 36.404 uVrms**)

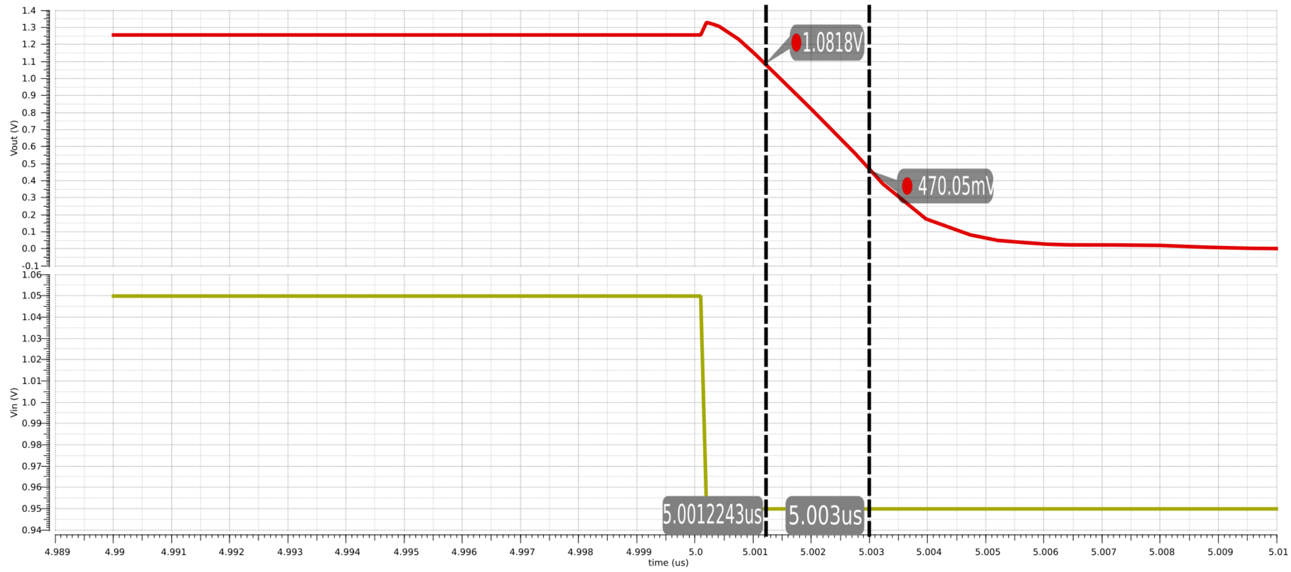
```
Device    Param    Noise Contribution    % Of Total

/I22/M2   id       0.000298045           27.29
/I22/M1   id       0.000298045           27.29
/I22/M4   id       0.000205459           12.97

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000570528
Total Input Referred Noise = 3.64035e-05
The above noise summary info is for noise data
```

Large Signal Step Response (Slew rate measurement)

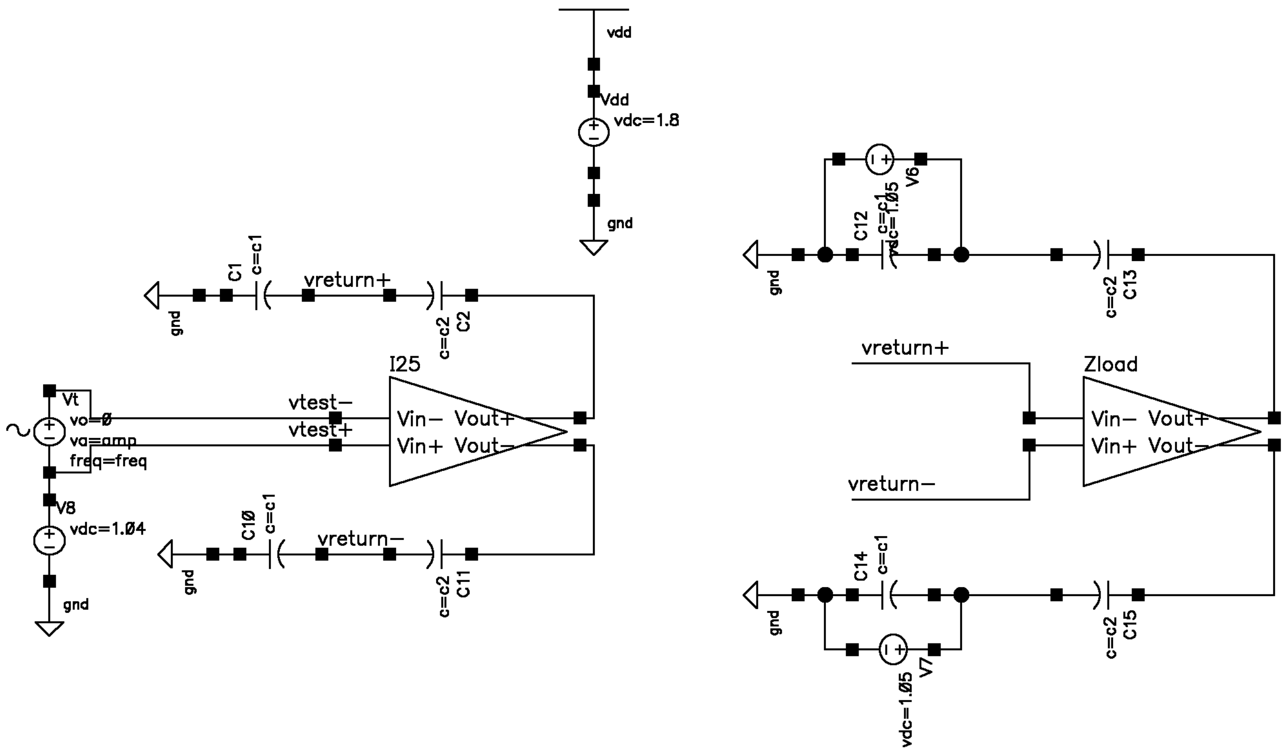
For the slew rate measurement a 100mV input differential pulse was applied, and the opamp slewing was measured at the output in the linear region:



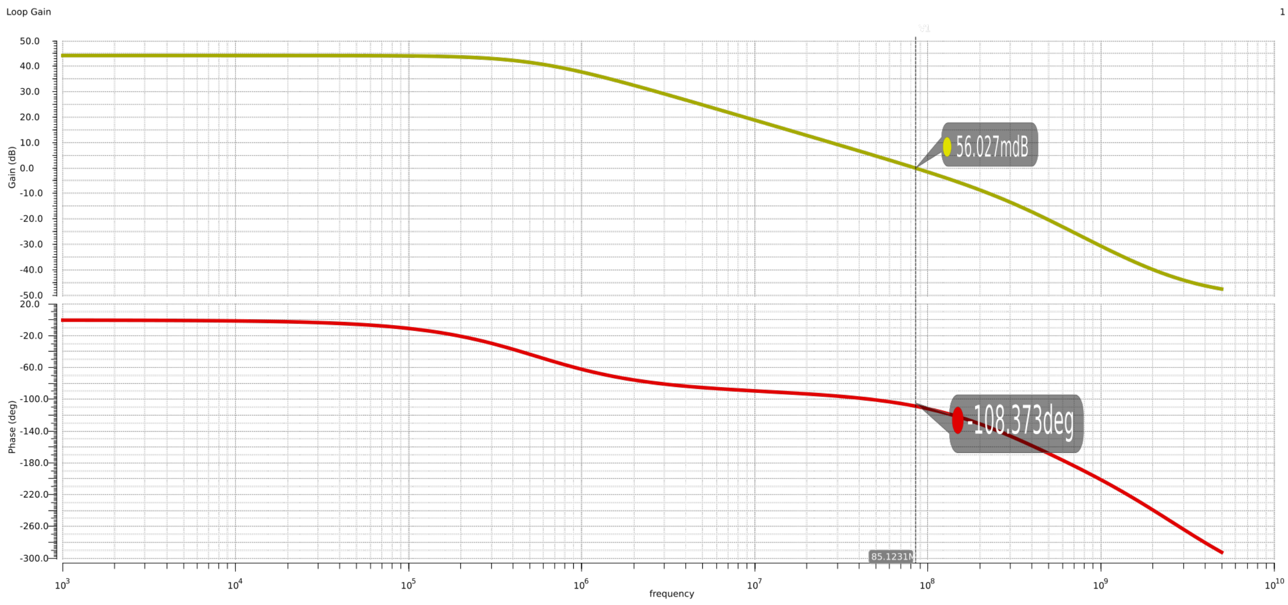
Slew Rate: $SR = \frac{470.05\,mV - 1.0818\,V}{5.003\,uS - 5.0012243\,uS} = -344.51\,\frac{V}{uS}$

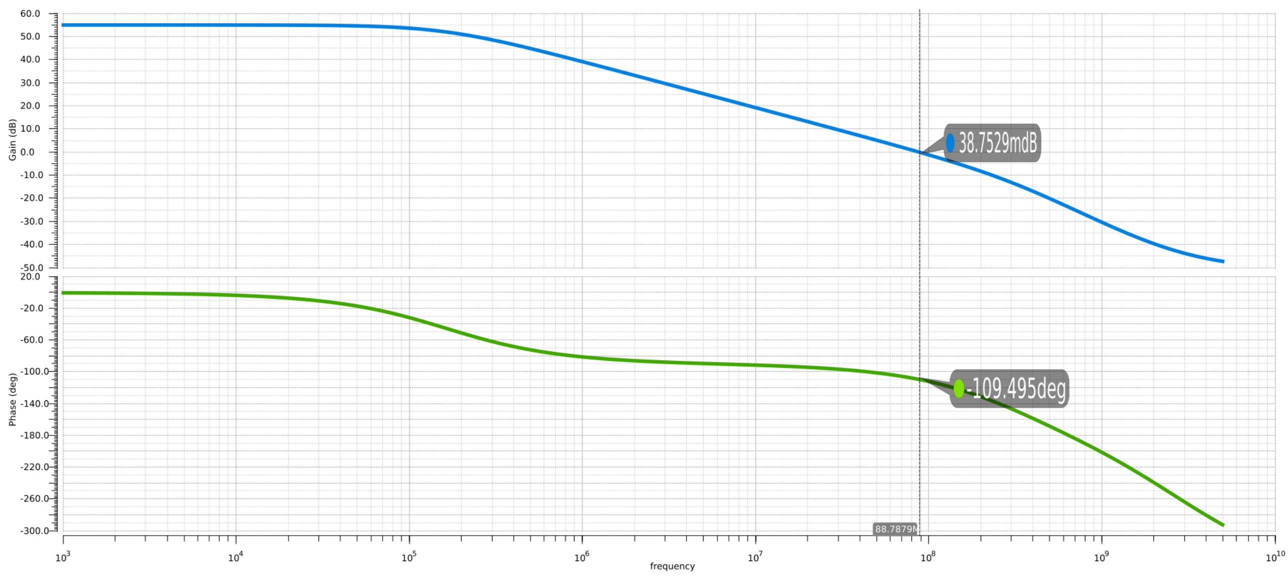
Fully-differential Open Loop Response Results

The open-loop measurement utilized for this section was as follows (with self-loading Zload applied at Vreturn):



The bode-plot and phase-margin obtained from our open-loop testbench can be found below (both for maximum gain and minimum gain cases):





The precise phase margin results are (max and min gain respectively)

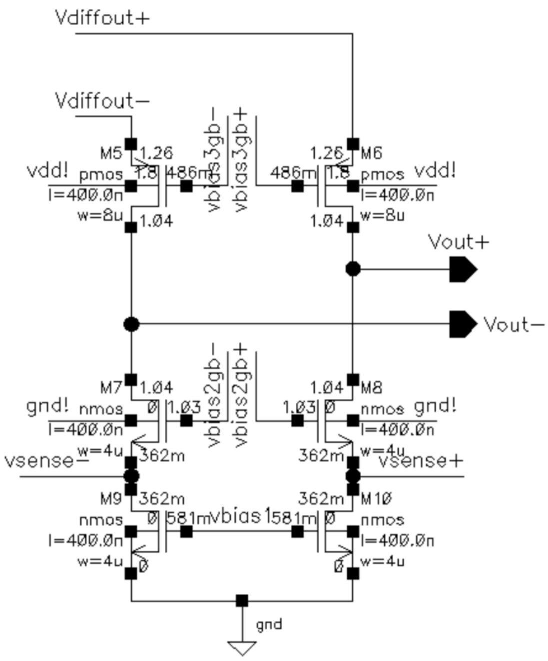
Phase Margin	71.52	Phase Margin	70.43

Upon measurement the min phase margin was found to be above the necessary 70 degrees.

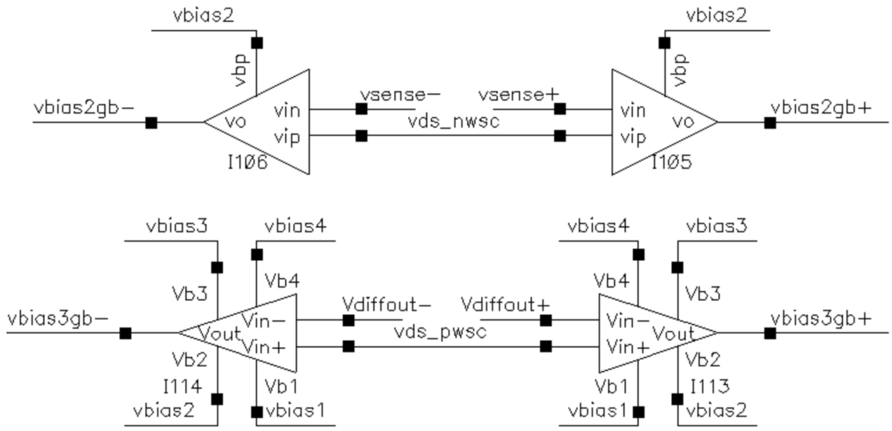
Gain Enhancement Results (to meet gain error spec)

To be able to meet the gain error spec, we opted to add gain boosting amplifiers to both of our NMOS and PMOS cascode transistors (as the sense inverting inputs to the opamp are close to the rails; in each case we need to use a PMOS input-pair and NMOS input-pair opamps). We are using the same single ended Opamp from this assignment (above) and the PMOS input-pair 2-stage Opamp from assignment 1, with the bias voltages provided through external pins we avoid the use of resistors as required. The new schematic blocks are as follows:

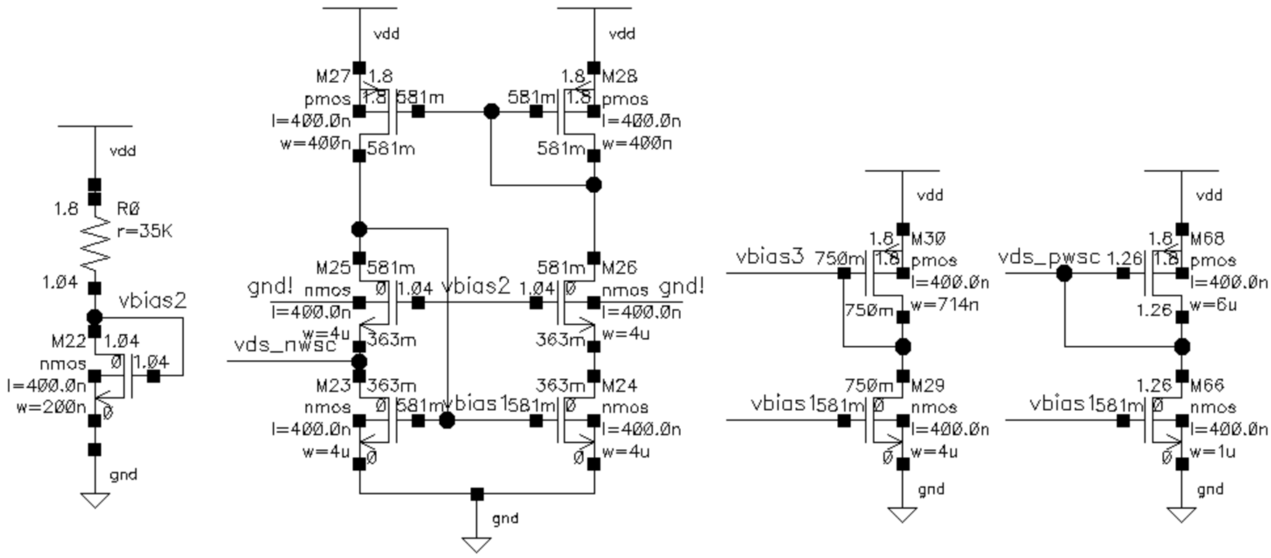
Output stage with cascode transistors and updated node voltages



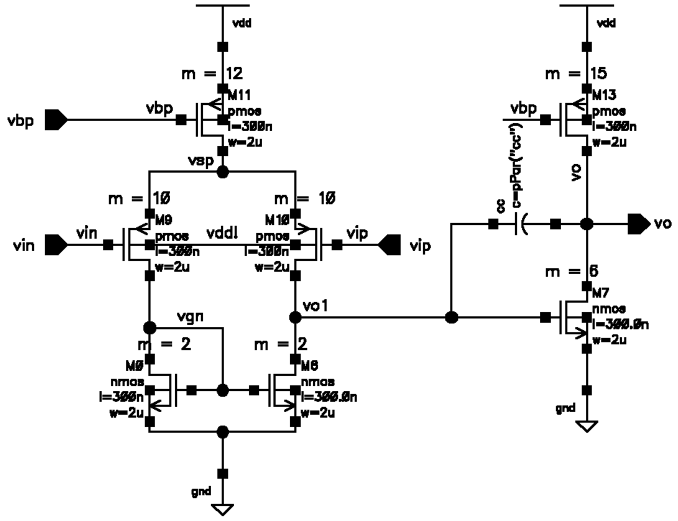
Additional single ended opamps added to enforce our desired Vds across the NMOS and PMOS current mirrors. (top are



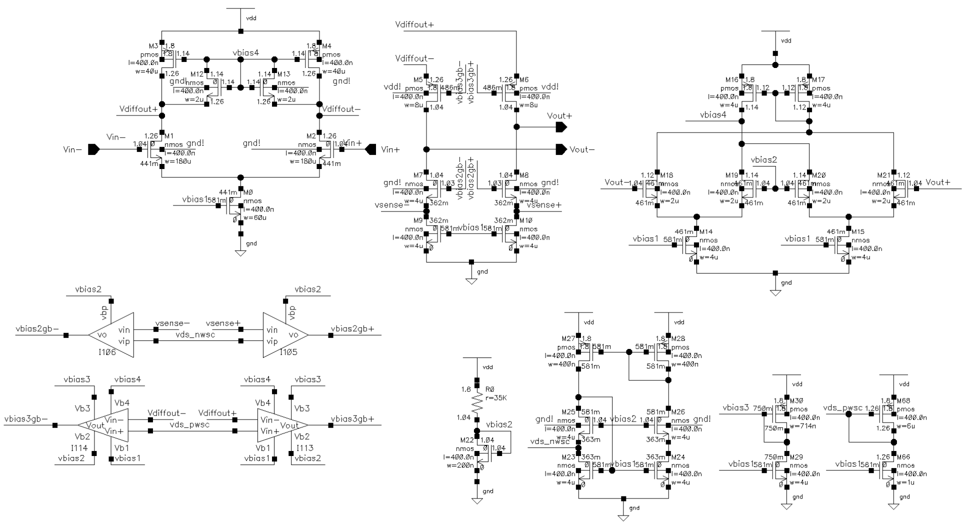
New bias circuits required to make use of the opamps without any internal resistors or dc sources



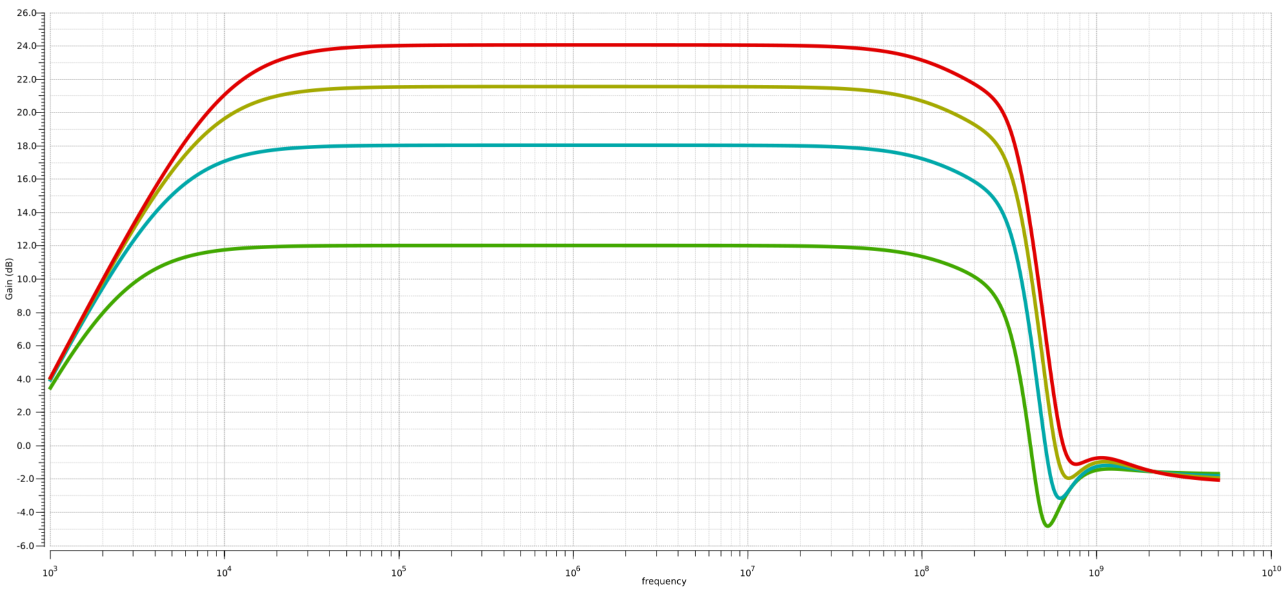
The schematics for the NMOS input-pair Opamp is the single-ended folded cascode design in the first section of this report, and the schematic for the PMOS input-pair 2-stage Opamp is displayed below:



The following is the complete schematic including all blocks



The following is the final gain plot for all gain settings (precise measurements below)



Precise results (4x gain)

DC Gain	12.04
Loop Gain Magnitude	wave
-3DB Bandwidth	259.9M

Precise results (8x gain)

DC Gain	18.06
Loop Gain Magnitude	wave
-3DB Bandwidth	248.9M

Precise results (12x gain)

DC Gain	21.58
Loop Gain Magnitude	wave
-3DB Bandwidth	245.5M

Precise results (16x gain)

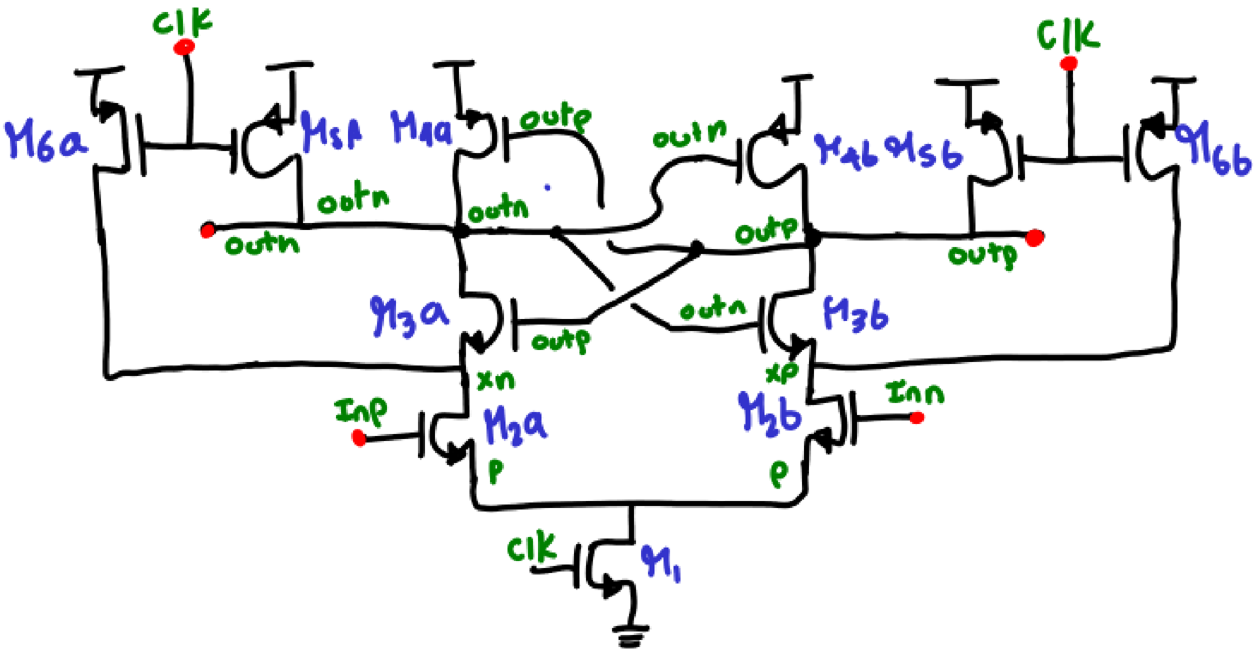
DC Gain	24.08
Loop Gain Magnitude	wave
-3DB Bandwidth	243.6M

Note the Cadence calculator approximates to two decimal places. In this, case the results are within the 0.25% gain error spec.

The complete list of devices with their saturation operating points (except slew-rate helpers) can be found in the appendix.

Part 2

The comparator described in the netlist is the Strong-Arm comparator.



To analyze the operation of the comparator we first analyze what happens at each clock phase:

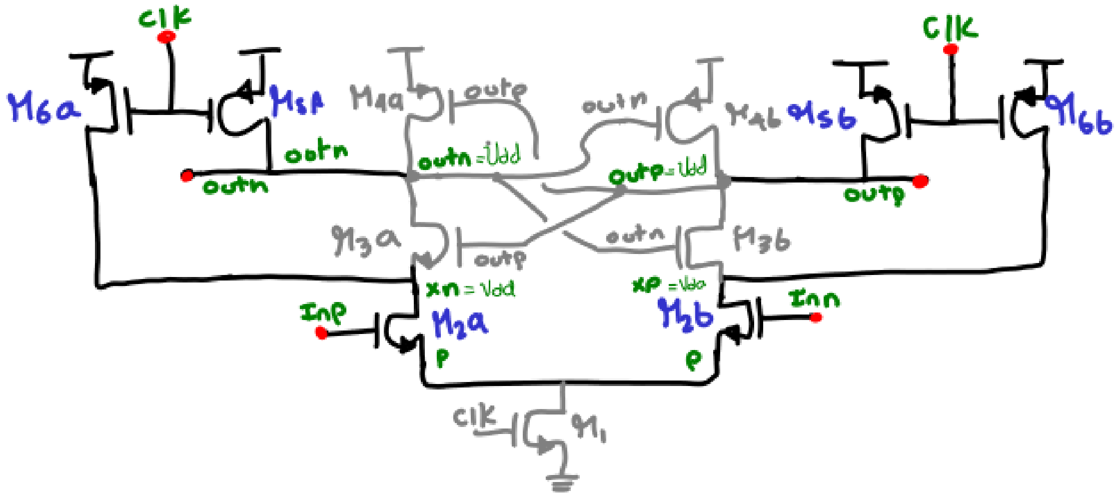
- Identify reset phase
- Identify initial condition after reset
- Analyze transient circuit operation until setpoint is reached.

Reset Phase: From the schematic we can see that the reset phase is when the clock goes low (i.e. reset=nclk)

In this case, on reset (clock low) we have:

- M6A,B and M5A,B act as reset switches and set : outn,p=Vdd and xn,p=Vdd.
- M3A,B also turns off as Vgs goes to 0V shortly thereafter
- M1 is switched off and node P slowly increase up to Vdd
  - Eventually M2A,B also turns Off

Therefore we have the starting condition of the comparator (initial condition after reset):



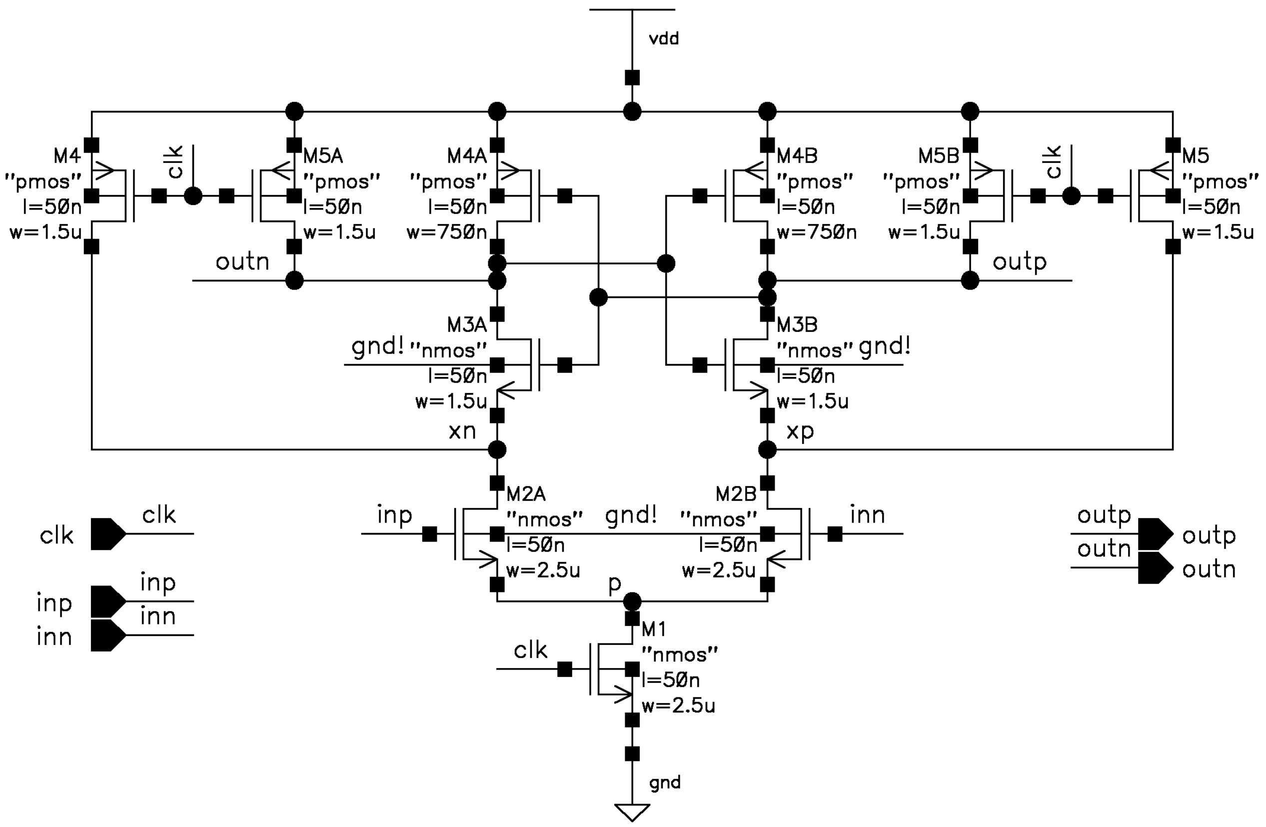
Comparison Phase: After clock goes high the comparison phase starts.

The process starts as soon as M1 turns on: node p starts decreasing, leading to M2A,B to start turning ON. *Note that as Inp > Inn, more current will ten to flow through M2A and M2B. (this tilts the balance of the loop)*

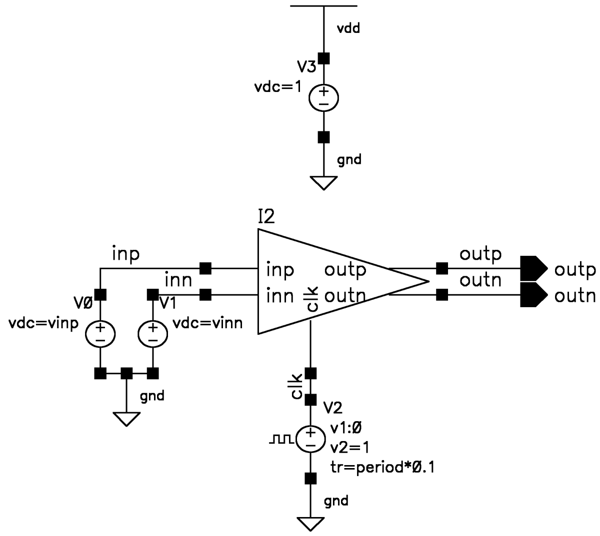
Node xn will be decreasing faster than node xp (due to larger branch current) in a “race to the bottom”. In turn, outn will decrease faster, decreasing both M3b and M4b gate voltages, this presents a positive feedback loop whereas M3B is driven weaker and weaker and starts carrying less and less current which together with M4B turning increasingly ON leads to an increase in outp node voltage; leading then to M3A turning further ON and M4A to start turning OFF.

The positive feedback process then continues until a stable condition is reached at each node close to the supply rails: outn close to 0V and outp close to Vdd.

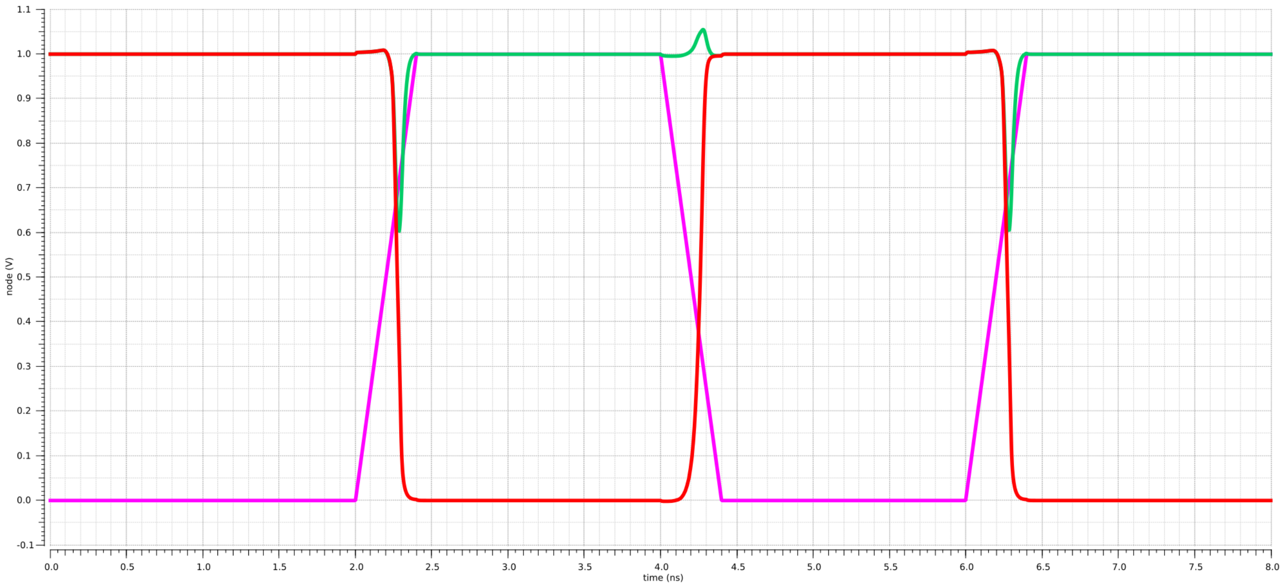
It is the starting condition set by Inp-Inn that determines the different in branch currents and thereafter the speed at which the output nodes reach the supply rails. (the propagation time, or time to latch). The complete comparator schematic is:



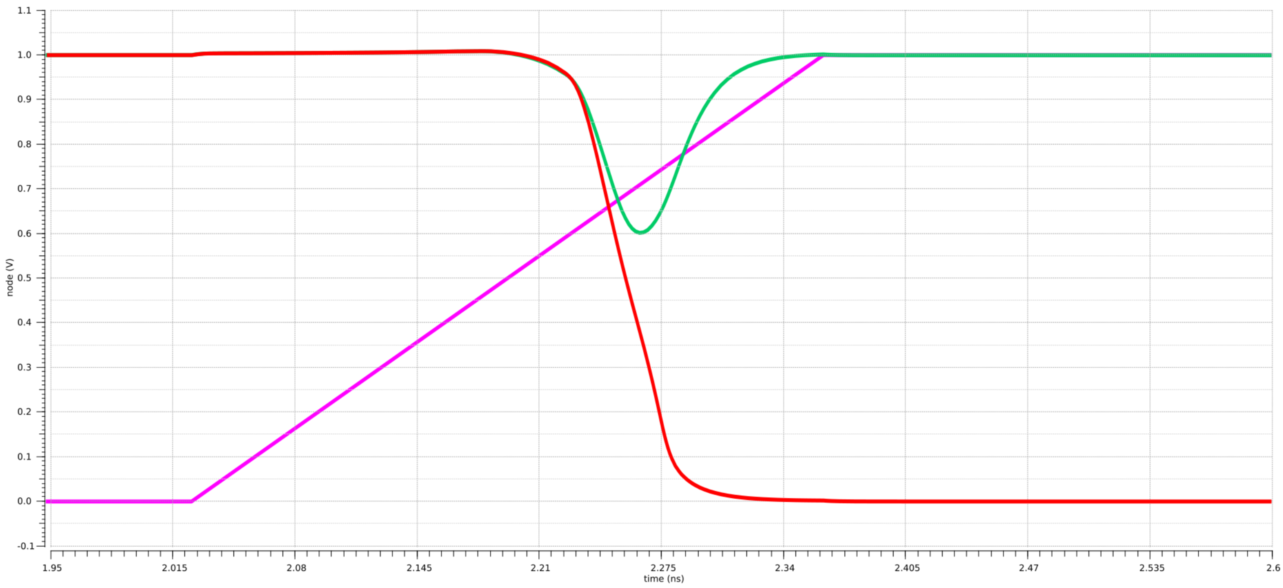
The initial operation of the comparator is assessed with the following testbench:



The following are the reset and compare phases

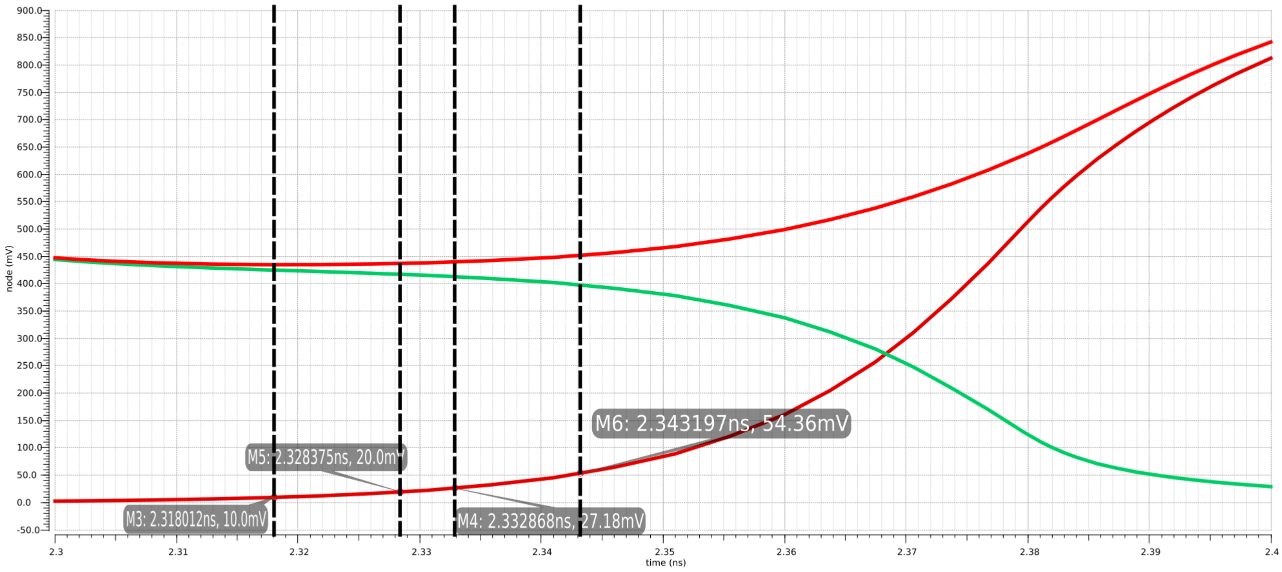


And the following is a close-up of the regeneration and positive feedback process



Regeneration Time Constant

The measurement of the regeneration time constant can be done by *applying a small 50uV* input and looking at the differential output waveform during the regeneration phase, specifically (reference [2] slides 10-16):



In this case $\tau = t_2 - t_1$ where t1: time at Voutdiff=10mV, and t2: time at Voutdiff=27.18mV.

should be similar or equal to:

$\tau = t_4 - t_3$ where t3: time at Voutdiff=20mV, and t3: time at Voutdiff=54.36mV.

Almost always if the Tau's are not very close in value, the problem is that the comparator has offset or hysteresis.

In our case, we have $\tau = 2.332868\,nS - 2.318012\,nS = 14.856\,pS$ and the other $\tau = 2.43197\,nS - 2.328375\,nS = 1.4822\,pS$

These time constants are very close indicating that the comparator will most-likely have very small offset or comparator errors.

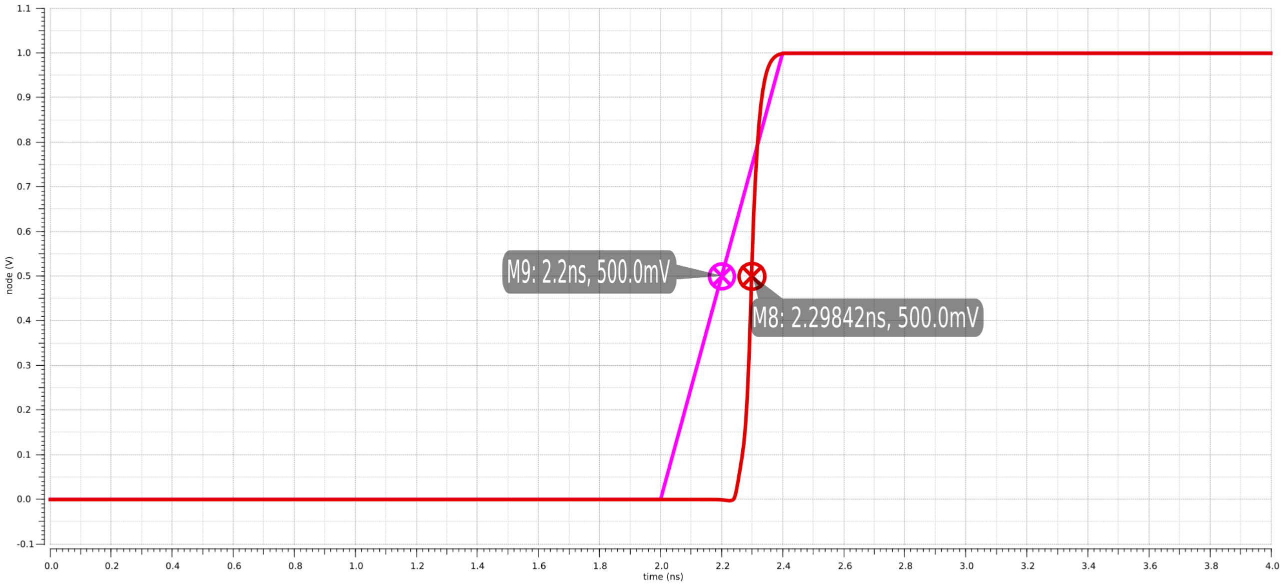
Propagation Delay (for 10mV input)

We can measure the large signal propagation delay by overdriving the input with a large signal and measure delay from clock input to output[2].

More formally propagation delay is defined as the difference between the moment the input signal crosses the reference voltage and the moment the output stage changes (usually when the output signal crosses 50% of Vdd if nothing is specified) [3]

This is one of the most important performance metrics denoting how quickly a comparator can resolve an applied input (see plot below)

In this case the propagation delay is: $T_{pd} = 2.29842\,nS - 2.2\,nS = 98.42\,pS$



Energy Consumed per Comparison (Fclk=250MHz)

Energy per conversion is a measure of the efficiency of the comparator at our operating frequency, and is defined canonically as: $E_{conv} = \frac{P}{F_{clk}}$ Assuming a differential input voltage of 10mV, a set clock frequency of 250MHz, and an average current consumption of 8.490uA (averaged over one transient simulation), we can estimate: $E_{conv} = \frac{(8.490 uA \, x \, 1 \, V)}{250 \, MHz} = 33.976 \frac{fJ}{conversion}$

Note this figure is small because our comparator is measured without the capacitive loading of the next stage which will increase significantly the current consumption of the comparator.

Sensitivity (when operated at a clock frequency of 100MHz)

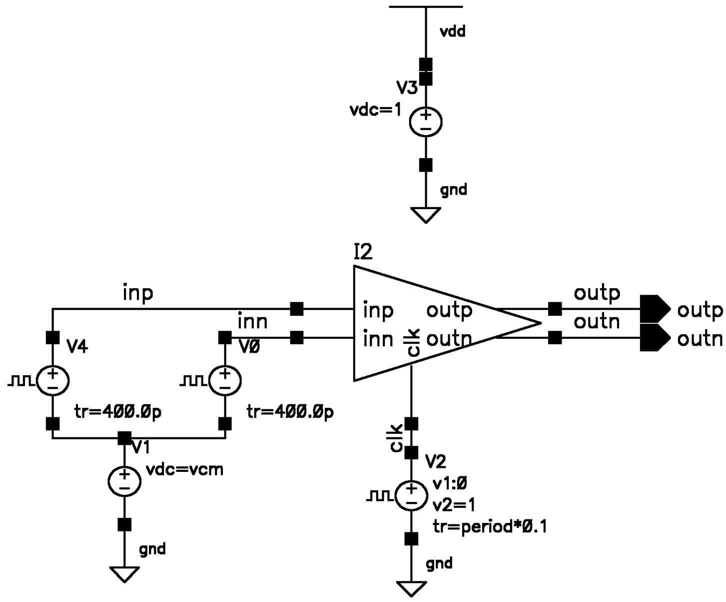
is the minimum input voltage that produces a consistent output, i.e. the smallest input that can be resolved and results in a decision latched at the output: this is also referred to as input offset.

The Iscas reference paper [2] reports an efficient simulation measurement for calculating comparator input offset, the process is as follows:

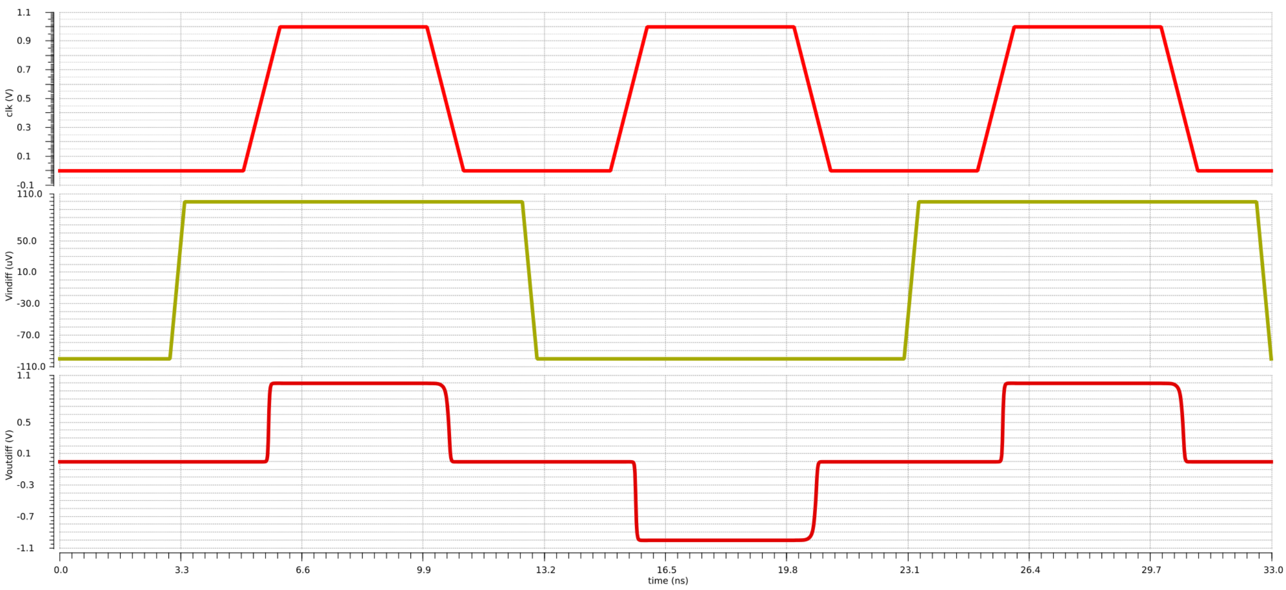
For this simulation measurement test-bench: we (1) apply a differential input to the comparator (100uV), subsequently (2) we measure the difference between the out_p and out_n metastable node voltages using a transient simulation. (3) next using an eye diagram tool we plot the the differential output with a period of one cycle. (4) Using the eye diagram diagram we pick a region in time where the difference between both waveforms is within 20mV to 100mV (this represents the exponential rise region of the waveform).

The simulation testbench used is as follows (this is the same testbench used for hysteresis and offset):

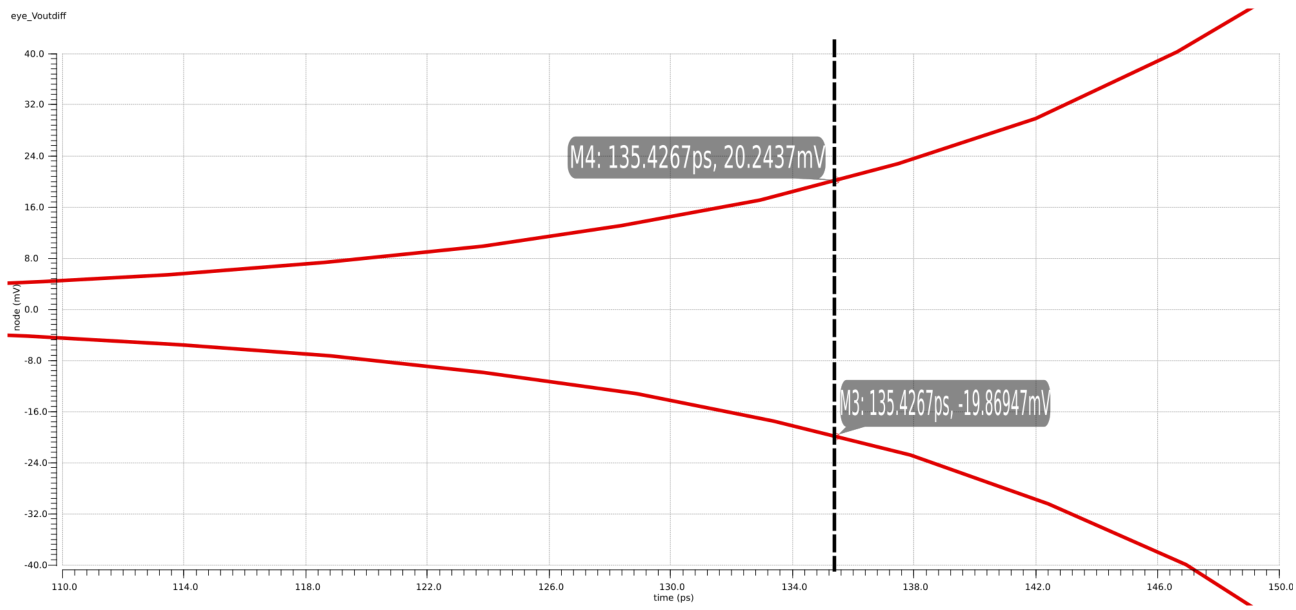
Initially we apply the recommended differential input square wave with +/-100uV



The offset simulation technique waveforms are applied as below



Subsequently we plot the eye diagram to find a two points with a difference of 20mV to 50mV



(note there is a visual-only artifact for the vector graphics exported from cadence)

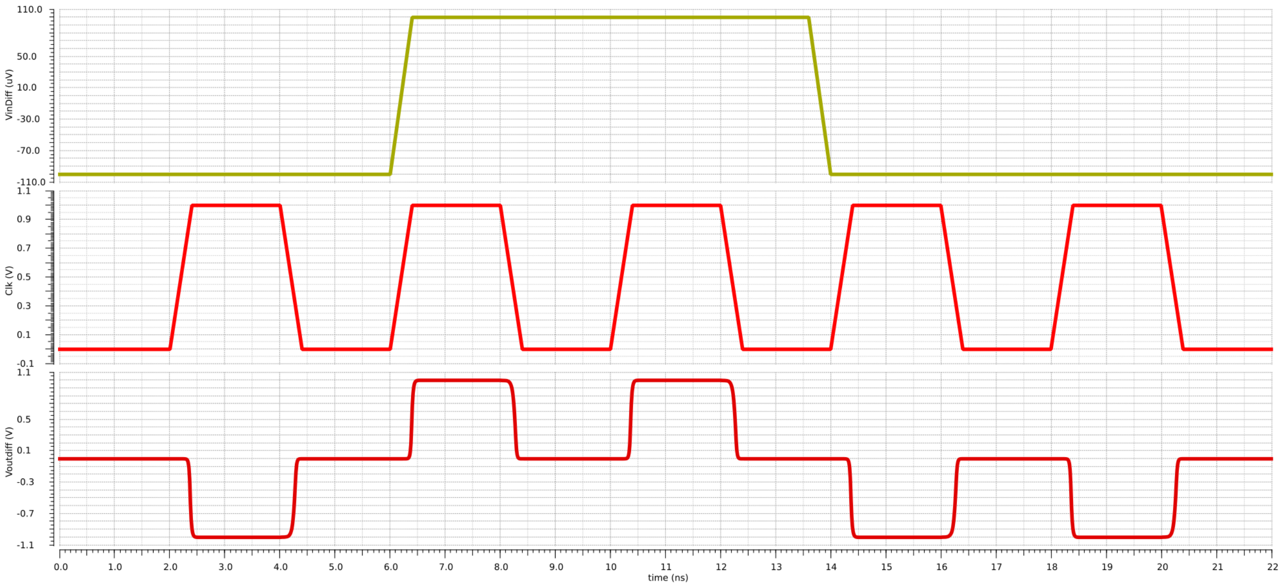
In this case $Gain = \frac{(V1 - V2)}{\Delta Vin} = \frac{20.2437\,mV - (-19.86947\,mV)}{200\,uV} = 200.57$ and we can calculate **the comparator offset** as = $Offset = \frac{-(V1 + V2)}{2x\,Gain} = \frac{-(20.2437\,mV - 19.86947\,mV)}{2x\,200.57} = -0.933uV$

This is a very small offset as hinted by the regeneration time constant calculation.

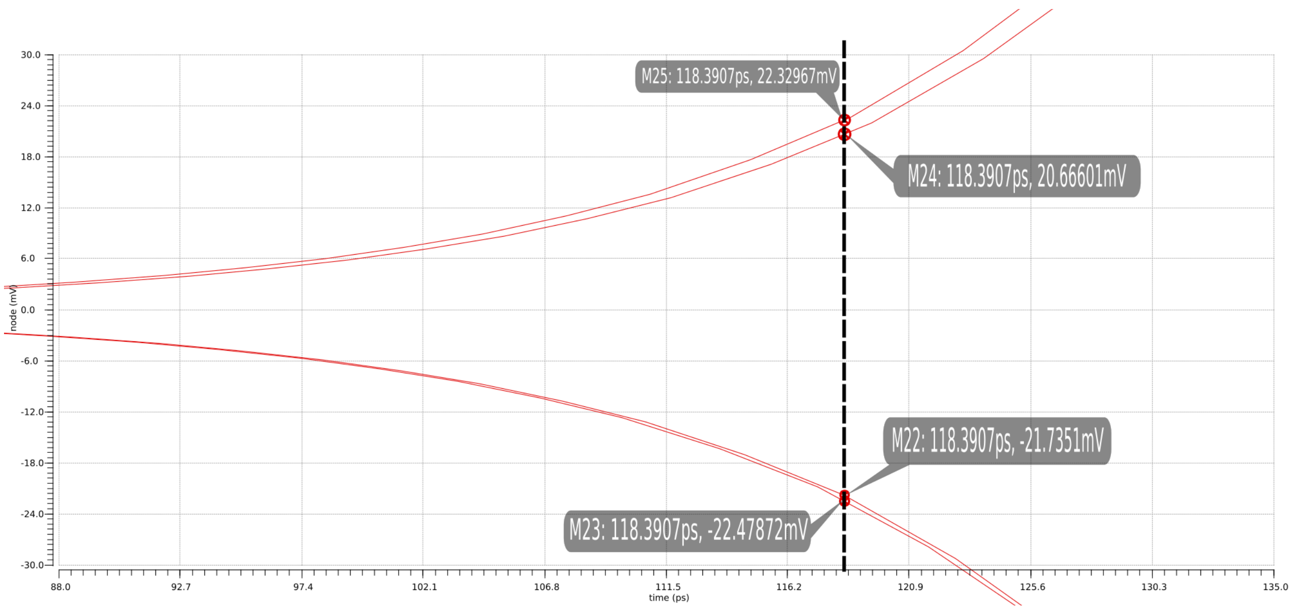
Hysteresis (nominal clock frequency of 250MHz)

Hysteresis is the normally undesirable memory effect of a comparator due to residual charge in nodes of the circuit (due to imperfect reset or kickback), whereby under an applied input when coming back from the opposite logic level the comparator trip-point differs from the ideal reference.

The Iscas reference paper mentions an efficient measurement procedure very similar to what we used for calculating the offset above, here we need only 5 clock cycles in order to be able to estimate our hysteresis as well as offset. The hysteresis simulation waveform is as follows (modeled exactly after the Iscas tutorial):



Subsequently we plot the eye diagram of the differential output



In this case: $Gain = \frac{(O3 - O4)}{\Delta Vin} = \frac{20.66601\,mV - (-22.47872\,mV)}{200\,uV} = 215.72$ and

Offset1 (V low to high sensitivity): $Offset\,1 = \frac{(O1 + O2)}{2\,x\,Gain} = \frac{597.57\,uV}{2\,x\,Gain} = 1.3781\,uV$

Offset2 (V high to low sensitivity): $Offset\,2 = \frac{(O3 + O4)}{2\,x\,Gain} = -4.2015\,uV$

We can then calculate hysteresis as:

Hysteresis: Offset1 – Offset2 = 5.5796uV

and average offset as: (Offset1 + Offset 2) / 2 = -1.412uV

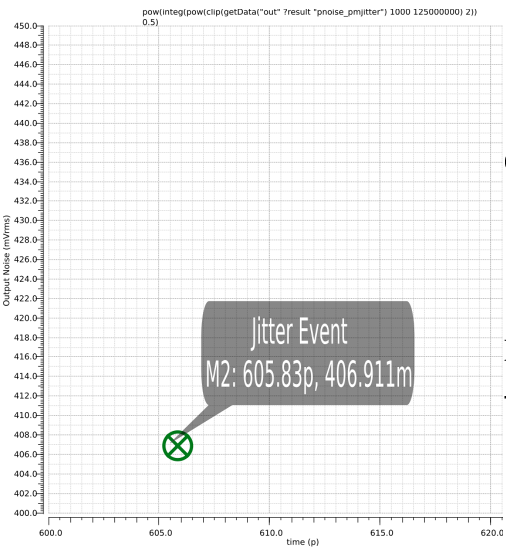
which is close to the comparator offset calculated before for a 100MHz clock.

Comparator Input Referred Noise

For the comparator noise analysis we are using the Periodic Steady State Analysis recommended in the ISCAS tutorial reference [2] as a better alternative to the standard transient noise simulation: simulation is faster and more accurate, displays sources of noise and allows us to select the noise bandwidth for integration.

The procedure outlined in the tutorial proceeds as follows: (1) apply a small DC input(100uV differential input), subsequently (2) clock comparator and measure noise in exponential region of rising vout differential waveform (we are choosing 50mV in our case). (3) we use the periodic steady state and Pnoise analysis choosing jitter for noise and setting a 50mV threshold to measure noise. (4) Finally we find the equivelent input referred noise by dividing the measured output noise by the calculated gain Voutdiff/Vindiff = 500.

We followed the detailed procedure from slide 57 to configure the pnoise and pss analyses being mindful over our 250MHz maximum clock frequency for our comparator. Subsequently we configured the direct plot form to add the expression to our outputs and finally (divide by our gain) to find our input referred noise.



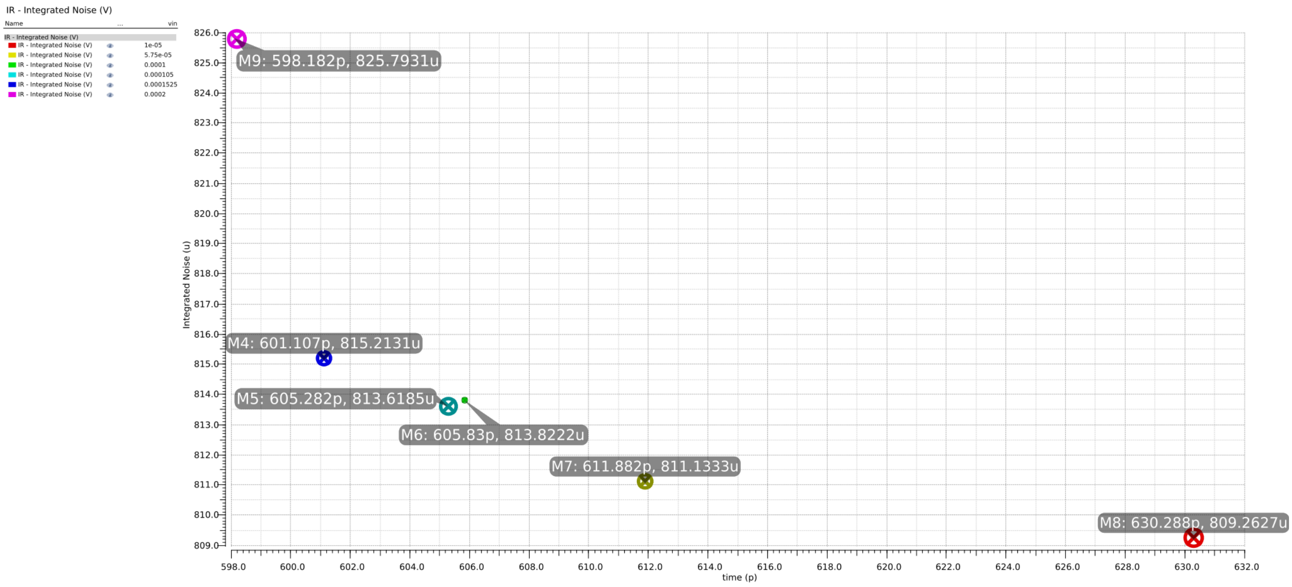
Output Integrated Noise: 406.911mVrms

Input-referred Integrated noise: 813.82uVrms

(integrated over 10K to 256MHz bandwidth)

In this case with a 100uV input and given our input offset of -1.412uV, we have a ~1.4% error in our noise measurement.

Finally we calculated the input referred noise for different input amplitudes (as exemplified in slide 52):



Here we can see that most values fall within 810 to 830uVrms, for smaller input values offset plays a more important role as % of error, at larger amplitudes the noise measurement technique starts to incur into other inaccuracies (as we leave the exponential region of the comparator differential output).

Discussion

In retrospect thinking back on our chosen topology and the large intrinsic gain necessary for the Opamp (to maintain the closed-loop gain error spec), it perhaps would have been simpler to pursue a 2-stage Opamp design with an inherently larger gain and requiring no extra gain-enhancing efforts as was required for the folded cascode Opamp.

References

[1] Design Procedures for a Fully Differential Folded-Cascode CMOS Operational Amplifier: https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=45013

[2] Dynamic Comparator Noise and Metastability Simulation Techniques (ISCAS 2017, William Evans)

[3] Introduction to comparators, their parameters and basic applications: https://www.st.com/content/ccc/resource/technical/document/application_note/group0/88/5b/0a/e2/7d/39/4e/9e/DM00050759/files/DM00050759.pdf/jcr:content/translations/en.DM00050759.pdf

[4] Notes on Gain Error: https://www.elexp.com/Images/Notes_on_Gain_Error_in_Op-Amp_Amplifiers.pdf

[5] Cascode Opamps (CMOS Analog Circuit Design): https://aicdesign.org/wp-content/uploads/2018/08/lecture24-170907.pdf

ERRATA

Note in part 2: the use of transistors as pseudo-resistors to generate references should be avoided as it incurs large variations in reference current with changes in power supply voltage.

Appendix

Operating point of transistors in fully-differential opamp with gain boosting.

subckt	xi20	xi20	xi20	xi20	xi20	xi20	xi20	xi20	xi20	xi20	xi20	xi20
element	1:m68	1:m30	1:m27	1:m28	1:m17	1:m16	1:m6	1:m5	1:m4	1:m3	1:m66	1:m25
model	0:pmos	0:pmos	0:pmos	0:pmos	0:pmos	0:pmos	0:pmos	0:pmos	0:pmos	0:pmos	0:nmos	0:nmos
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	-0.000005669	-0.00001995	-0.0000186	-0.0000186	-0.00001901	-0.00001893	-0.0000186	-0.0000186	-0.0001584	-0.0001584	0.000005669	0.0000186
vgs	-0.5422	-1.049	-1.219	-1.219	-0.6818	-0.6818	-0.7715	-0.7715	-0.6635	-0.6635	0.5809	0.675
vds	-0.5422	-1.049	-1.219	-1.219	-0.6818	-0.6635	-0.2192	-0.2192	-0.5422	-0.5422	1.257	0.2177
vth	-0.4539	-0.4383	-0.4248	-0.4248	-0.4525	-0.4525	-0.6088	-0.6088	-0.4554	-0.4554	0.4504	0.5615
vdsat	-0.0971	-0.4562	-0.5801	-0.5801	-0.1944	-0.1943	-0.1586	-0.1586	-0.1824	-0.1824	0.1118	0.1109
vod	-0.08832	-0.6115	-0.7943	-0.7943	-0.2293	-0.2292	-0.1626	-0.1626	-0.2081	-0.2081	0.1305	0.1135
gm	0.00008856	0.00005719	0.0000423	0.0000423	0.0001502	0.0001498	0.0001951	0.0001951	0.001381	0.001381	0.00008021	0.0002801

subckt	xi20	xi20	xi20	xi20	xi20	xi20	xi20	xi20	xi20	xi20	xi20	xi20
element	1:m26	1:m24	1:m23	1:m22	1:m15	1:m14	1:m21	1:m18	1:m10	1:m9	1:m19	1:m20
model	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	0.0000186	0.0000186	0.0000186	0.00002177	0.00001897	0.00001897	0.000009504	0.000009504	0.0000186	0.0000186	0.000009467	0.000009467
vgs	0.675	0.5809	0.5809	1.038	0.5809	0.5809	0.5777	0.5777	0.5809	0.5809	0.5772	0.5772
vds	0.2177	0.3632	0.3632	1.038	0.4609	0.4609	0.6573	0.6573	0.3619	0.3619	0.6756	0.6756
vth	0.5615	0.4594	0.4594	0.4396	0.4587	0.4587	0.4566	0.4566	0.4595	0.4595	0.4564	0.4564
vdsat	0.1109	0.1062	0.1062	0.3792	0.1066	0.1066	0.1059	0.1059	0.1062	0.1062	0.1057	0.1057
vod	0.1135	0.1215	0.1215	0.5985	0.1222	0.1222	0.1211	0.1211	0.1215	0.1215	0.1208	0.1208
gm	0.0002801	0.0002784	0.0002784	0.00006249	0.0002828	0.0002828	0.0001422	0.0001422	0.0002784	0.0002784	0.0001419	0.0001419

subckt	xi20	xi20	xi20	xi20	xi20	xi20	xi20	xi20	xi20.xi113	xi20.xi113	xi20.xi113	xi20.xi113
element	1:m8	1:m7	1:m13	1:m1	1:m12	1:m29	1:m2	1:m0	2:m6	2:m5	2:m4	2:m3
model	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:pmos	0:pmos	0:pmos	0:pmos
region	Saturati	Saturati	Cutoff	Saturati	Cutoff	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	0.0000186	0.0000186	-4.776E-16	0.0001398	-4.776E-16	0.00001995	0.0001398	0.0002797	-0.000008589	-0.000008595	-0.0001529	-0.0001529
vgs	0.6716	0.6716	-0.1213	0.5976	-0.1213	0.5809	0.5976	0.5809	-0.6562	-0.6569	-0.6635	-0.6635
vds	0.6768	0.6768	-0.1213	0.8168	-0.1213	0.7503	0.8168	0.4411	-0.9201	-0.8726	-0.3928	-0.3936
vbs	-0.3619	-0.3619	-1.257	-0.4411	-1.257	0	-0.4411	0	0.3936	0.3928	0	0
vth	0.5611	0.5611	0.7303	0.5818	0.7303	0.4565	0.5818	0.4594	-0.5669	-0.5669	-0.4559	-0.4559
vdsat	0.109	0.109	0.04233	0.06036	0.04233	0.108	0.06036	0.1062	-0.1047	-0.1052	-0.182	-0.182
vod	0.1105	0.1105	-0.8516	0.01581	-0.8516	0.1244	0.01581	0.1215	-0.08929	-0.09	-0.2076	-0.2076
gm	0.0002856	0.0002856	1.46E-14	0.003163	1.46E-14	0.0002931	0.003163	0.004183	0.0001304	0.0001302	0.001341	0.001342

subckt	xi20.xi113	xi20.xi113	xi20.xi113	xi20.xi113	xi20.xi113	xi20.xi113	xi20.xi113	xi20.xi114	xi20.xi114	xi20.xi114	xi20.xi114	xi20.xi114
element	2:m0	2:m10	2:m9	2:m8	2:m7	2:m1	2:m2	3:m6	3:m5	3:m4	3:m3	3:m0
model	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:pmos	0:pmos	0:pmos	0:pmos	0:nmos
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	0.0002886	0.000008589	0.000008595	0.000008589	0.000008595	0.0001443	0.0001443	-0.000008589	-0.000008595	-0.0001529	-0.0001529	0.0002886
vgs	0.5809	0.5345	0.5345	0.6425	0.6395	0.6391	0.6391	-0.6562	-0.6569	-0.6635	-0.6635	0.5809
vds	0.6187	0.3957	0.3987	0.0907	0.1358	0.7877	0.7884	-0.9201	-0.8726	-0.3928	-0.3936	0.6187
vth	0.4581	0.4592	0.4592	0.5696	0.5703	0.624	0.624	-0.5669	-0.5669	-0.4559	-0.4559	0.4581
vdsat	0.1071	0.07946	0.07947	0.08653	0.08448	0.06198	0.06197	-0.1047	-0.1052	-0.182	-0.182	0.1071
vod	0.1229	0.07531	0.07533	0.07294	0.0692	0.01513	0.01512	-0.08929	-0.09	-0.2076	-0.2076	0.1229
gm	0.004282	0.0001601	0.0001602	0.0001498	0.0001601	0.003285	0.003284	0.0001304	0.0001302	0.001341	0.001342	0.004282

subckt	xi20.xi114	xi20.xi114	xi20.xi114	xi20.xi114	xi20.xi114	xi20.xi114	xi20.xi106	xi20.xi106	xi20.xi106	xi20.xi106	xi20.xi106	xi20.xi106
element	3:m10	3:m9	3:m8	3:m7	3:m1	3:m2	4:m7	4:m6	4:m0	4:m13	4:m11	4:m10
model	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:pmos	0:pmos	0:pmos
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	0.000008589	0.000008595	0.000008589	0.000008595	0.0001443	0.0001443	0.0003399	0.0001303	0.0001307	-0.0003399	-0.000261	-0.0001303
vgs	0.5345	0.5345	0.6425	0.6395	0.6391	0.6391	0.7168	0.7421	0.7421	-0.7618	-0.7618	-0.8522
vds	0.3957	0.3987	0.0907	0.1358	0.7877	0.7884	1.033	0.7168	0.7421	-0.7665	-0.5846	-0.4986
vth	0.4592	0.4592	0.5696	0.5703	0.624	0.624	0.4651	0.4678	0.4676	-0.4612	-0.4618	-0.6226
vdsat	0.07946	0.07947	0.08653	0.08448	0.06198	0.06197	0.1886	0.202	0.2021	-0.2459	-0.2454	-0.2085
vod	0.07531	0.07533	0.07294	0.0692	0.01513	0.01512	0.2517	0.2743	0.2745	-0.3007	-0.3	-0.2296
gm	0.0001601	0.0001602	0.0001498	0.0001601	0.003285	0.003284	0.002512	0.000875	0.0008767	0.001992	0.001544	0.0009985

subckt	xi20.xi106	xi20.xi105	xi20.xi105	xi20.xi105	xi20.xi105	xi20.xi105	xi20.xi105	xi20.xi105
element	4:m9	5:m7	5:m6	5:m0	5:m13	5:m11	5:m10	5:m9
model	0:pmos	0:nmos	0:nmos	0:nmos	0:pmos	0:pmos	0:pmos	0:pmos
region	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati	Saturati
id	-0.0001307	0.0003399	0.0001303	0.0001307	-0.0003399	-0.000261	-0.0001303	-0.0001307
vgs	-0.8535	0.7168	0.7421	0.7421	-0.7618	-0.7618	-0.8522	-0.8535
vds	-0.4733	1.033	0.7168	0.7421	-0.7665	-0.5846	-0.4986	-0.4733
vbs	0.5846	0	0	0	0	0	0.5846	0.5846
vth	-0.6227	0.4651	0.4678	0.4676	-0.4612	-0.4618	-0.6226	-0.6227
vdsat	-0.2094	0.1886	0.202	0.2021	-0.2459	-0.2454	-0.2085	-0.2094
vod	-0.2308	0.2517	0.2743	0.2745	-0.3007	-0.3	-0.2296	-0.2308
gm	0.0009973	0.002512	0.000875	0.0008767	0.001992	0.001544	0.0009985	0.0009973