Part 1

For part I, we are asked to construct the current mirror as specified in the schematic from the lab write-up, with a a bias current of 50uA, a load voltage at the drain of Q2 of 600mV and transistor sizes in a 1:1 ratio (leading to a respective 1:1 current ratio).

Furthermore we are asked to select transistor sizes so as to guarantee the matching in output current stays within +/- 2% of it's set-point even under a 3σ random mismatch between our mirror transistors Q1 and Q2.

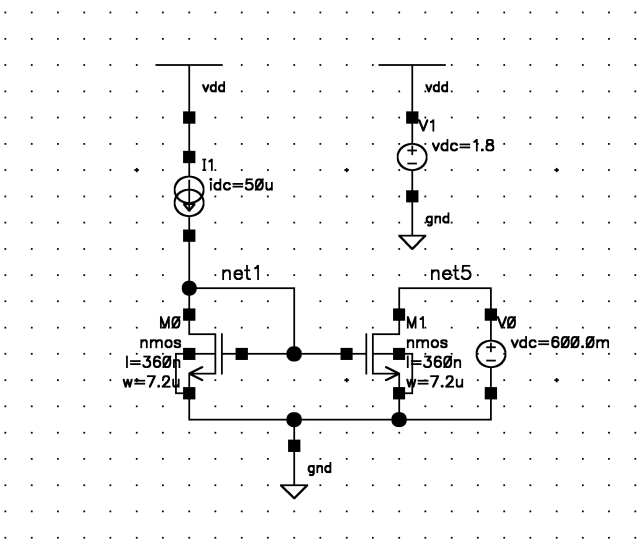
Note: we will be using HSPICE within a Cadence environment (See class resources: HSPICE Quick Start and [1]). We will be using the schematic entry editor in order to draw our circuit schematic and assign the appropriate device parameters, and the analog design environment (ADE) – with the HSPICE simulator selected and the given 180nm CMOS models – in order to generate our SPICE netlists and subsequently simulate our circuit using HSPICE. From my past experience, it is very easy to mis-assign (or swap) nets when writing SPICE netlists by hand, often leading to unnecessary time spent debugging, hence I often try to use schematic entry software for this purpose. Exported schematics and plots will be post-processed (GIMP, Inkscape) for readability and to highlight important results.

To size the NMOS transistors appropriately (given λ = f/2, and f = 180nm), a common starting point is to size our unit transistor as: $\frac{W}{L}=\frac{4L_{min}}{2L_{min}}=\frac{8\lambda}{4\lambda}=\frac{8(90\,nm)}{4(90\,nm)}=\frac{720\,nm}{360\,nm}$ and subsequently, resize the width of our transistors to arrive at our desired specs.

In our case, initially with our initial dimensions, the output currents are: $I_i=50\,\mu A$ $I_o=48.708\,\mu A$

The discrepancy in output current arises due to the different in drain voltages at the outputs of both MOSFETs which leads to different horizontal fields that create channel length modulation effects. In our case, to equalize the drain currents we need to have the same potential applied to the drain of both mosfets (600mV), we can accomplish this by increasing the transistors width (decreasing Veff i.e. Vds for Q1) so as to decrease both Vds to 600mV. An optimization parametric sweep reveals an optimal W=7.459µ, which leads to identical matched currents, however **choosing a practical integer multiple of Lmin results in a viable W=7200nm, a 20 unit (m=20) transistor:** $\frac{W}{L}=\frac{7200\,nm}{360\,nm}=20$ **where our currents:** $I_i=49.949\,\mu A$ $I_o=49.98\,\mu A$

The current mirror circuit schematic with clearly annotated device sizes is (exported schematic was post-processed for clarity):



Where:

Idc = 50µA

Vload = 600mV

W1,2 = 7.2µm

L1,2 = 360nm

Vsupply = 1.8V

The netlist used for nominal simulation was:

```
*** Project 1: Part 1 (current mirror netlist) ***
* ---
* Includes: models
* ---
.INCLUDE "project_1/p18_models/p18_cmos_models_tt.inc"

* ---
* Hspice options
* ---
.OPTION post

* ---
* Variable parameters
* ---
.PARAM nlength=360n nwidth=7200n

* ---
* Global nets
* ---
.GLOBAL vdd!

* ---
* Netlist
* ---
* dev   <nets>          <values>
* ------------------------------
i1      vdd! net1       DC=50e-6
v1      vdd! 0          DC=1.8
v0      net5 0          DC=600e-3
m1      net5 net1 0 0   nmos L=nlength W=nwidth
m0      net1 net1 0 0   nmos L=nlength W=nwidth

* ---
* Simulation Testbench
* ---
.TEMP 25.0
.OP
.TRAN 1e-9 100e-9 START=0.0

* ---
* Outputs
* ---
.PRINT I(m1) I(m0)
.END
```

And the operating point results:

```
******  operating point information      tnom=  25.000 temp=  25.000
***** operating point status is all       simulation time is     0.
    node    = voltage      node      = voltage      node      = voltage
 +0:net1    = 602.4148m    0:net5    = 600.0000m    0:vdd!    =   1.8000

 ****  voltage sources

 subckt
 element  0:v1       0:v0
  volts      1.8000   600.0000m
  current  -50.0000u  -49.9790u DC Operating Point
```

And the transistor operating points and region from the SPICE simulation (most important parameters in bold)

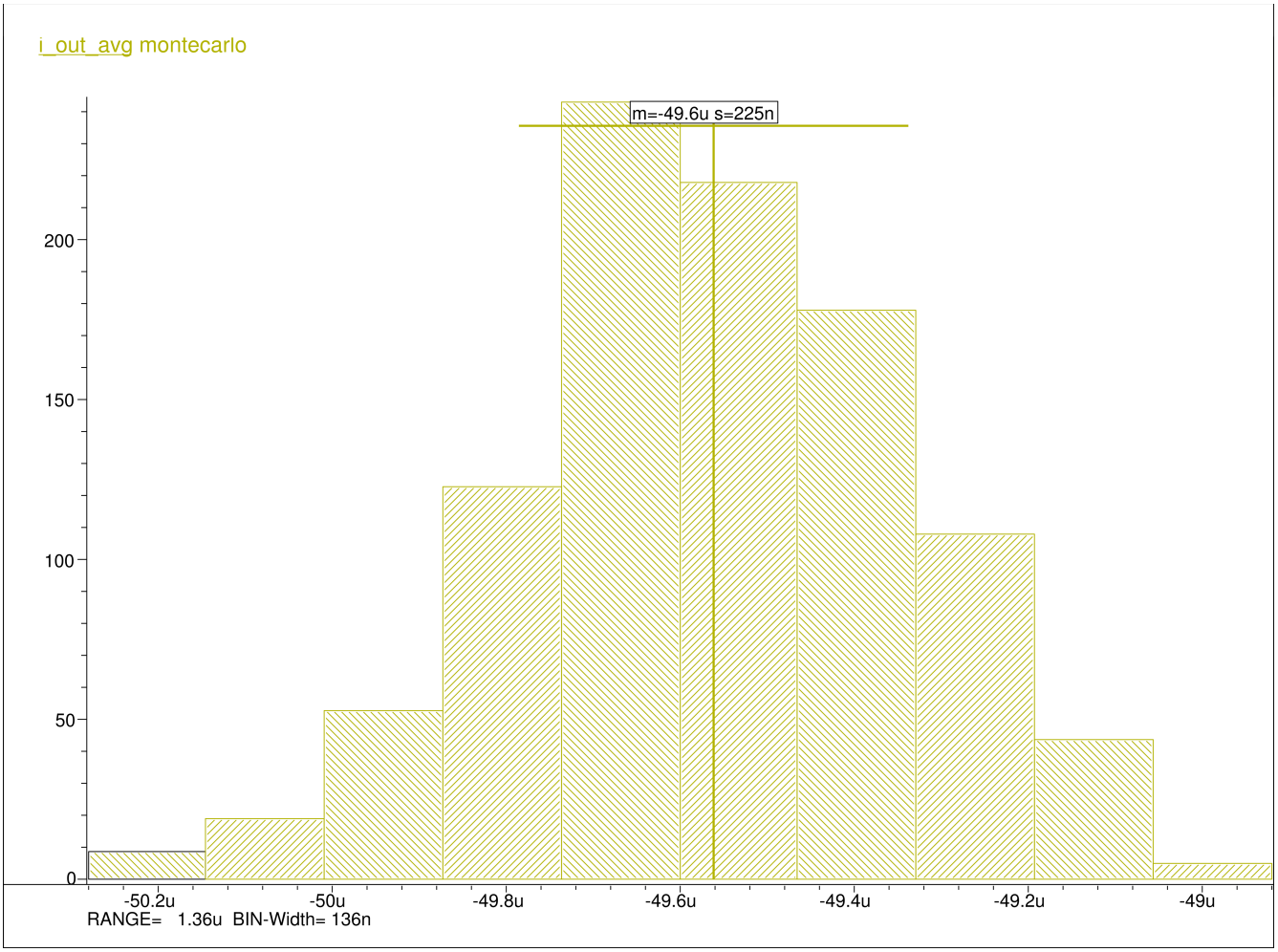
```
 element  0:m1       0:m0
 model    0:nmos     0:nmos
 region   Saturati   Saturati
  id      49.9790u   50.0000u
  ibs     0.         0.
  ibd     0.         0.
  vgs     602.4148m  602.4148m
  vds     600.0000m  602.4148m
  vbs     0.         0.
  vth     463.1112m  463.0924m
  vdsat   117.7572m  117.7693m
  vod     139.3036m  139.3224m
  beta    6.3677m    6.3677m
  gam eff 575.8477m  575.8477m
  gm      675.8740u  676.0694u
  gds     8.6986u    8.6911u
  gmb     1.1588m    1.1631m
  cdtot   4.9639f    4.9638f
  cgtot   26.0705f   26.0705f
  cstot   22.4353f   22.4724f
  cbtot   208.9232a  189.3239a
  cgs     43.1185f   43.2123f
  cgd     4.8894f    4.8893f
```

The main important items to notice, is that as desired both of our transistors drain voltages are close to 600mV (2mV difference due to integer size chosen for device's width) leading to well matched currents, and the transistors are operating in the saturation/active region as expected.

Now we needed to make sure the maximum allowed deviation from our setpoint is +/- 2% or: 50x0.02 = +/- 1µA over a 3σ random mismatch monte-carlo simulation.

In our case a transient analysis was set in place for 100nS, then a montecarlo simulation was setup to run for 1000 runs, given 3σ max variations for specific M1 and M2 model parameters. Finally to get a good estimate of the output current, a measurement command was used to average the total output current points for every run.

For plotting, the HSPICE generated data was imported into SPICE explorer and a **histogram waveform was used to display the statistical variation of our output current with device mismatch.** (see the histogram on next page)



From our histogram we can see (negative sign, due to current measurement at supply positive terminal omitted): $I_{mean} = 49.6\,\mu A$ $\sigma = standard\ deviation = 0.225\,\mu A$ $\sigma^2 = variance = 0.0506\,\mu A^2$

$I_{range} = 1.36\,\mu A = \pm 0.68\,\mu A$

In our case, **the maximum deviation from the mean (worst case) is captured by the range of our data, which accounts for a +/- 0.68µA worst case variation under miss-match, hence our current mirror meets our required specifications of a max variation of +/- 1µA under mismatch.**

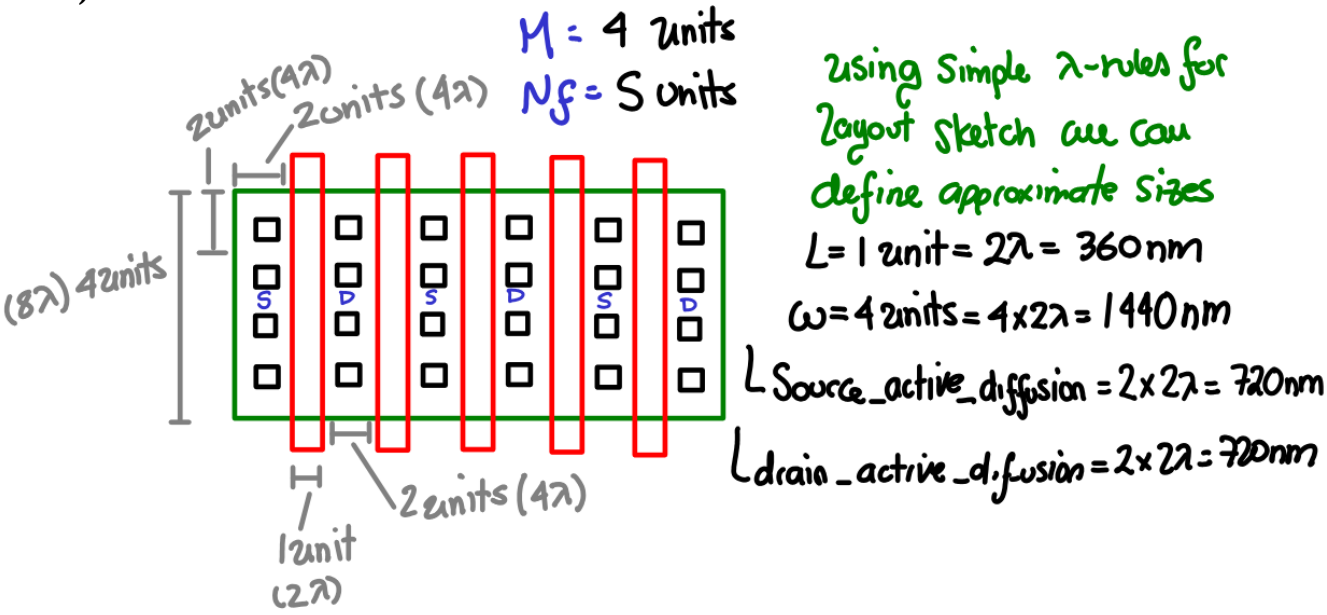
See the modified SPICE deck for montecarlo simulation below:

```
* Project 1: Part 1-b (current mirror netlist with montecarlo simulation)
* ===

* ---
* Includes: models
* ---
* .INCLUDE "project_1/p18_models/p18_cmos_models_tt.inc"

* ---
* Hspice options
* ---
.OPTION post

* ---
* Variable parameters
* ---
.PARAM nlength=360n nwidth=7560n

* ---
* Global nets
* ---
.GLOBAL vdd!

* ---
```

```
* Subcircuits definitions
* ---
*       dev    <nets>    <values>
* ------------------------------
.SUBCKT nmosmc d g s b  width=nwidth length=nwidth

.INCLUDE ../../mc_models/p18_model_card.inc
.PARAM sigma_vt_shift = '3.6e-15 / sqrt(width*length) + 1e-3'
.PARAM sigma_proc_delta = '1.8e-15 / sqrt(width*length) + 5e-4'
.PARAM proc_delta = agauss(1,'3*sigma_proc_delta',3)
.PARAM vt_shift = agauss(0,'3*sigma_vt_shift',3)
m1 d g s b NMOS (w = 'width' l = 'length')

.ends

* ---
* Netlist
* ---
* dev   <nets>          <values>
* ------------------------------
i1      vdd! net1       DC=50e-6
v1      vdd! 0          DC=1.8
v0      net5 0          DC=600e-3
x1      net5 net1 0 0   nmosmc L=nlength W=nwidth
x0      net1 net1 0 0   nmosmc L=nlength W=nwidth

* ---
* Simulation Testbench
* ---
.OP
.TRAN 1e-9 100e-9 START=0.0  sweep monte=1000

* ---
* Outputs
* ---
.MEAS TRAN i_out_avg AVG I(V0) FROM=0 TO=100nS
.PRINT I(V0)

.END
```

For the next question, we are asked to provide a layout sketch for the mirror and calculate estimates of the source/drain junction areas and perimeters for each transistor.

Given our 20/1 units transistor specified above $\frac{W}{L}=20/1=\frac{7200\,nm}{360\,nm}=\frac{40\,\lambda}{2\,\lambda}$ we can divide the layout into $M=\#\text{ of devices in parallel}=4$ and $N_f=\#\text{ of gate fingers}=5$ for a **layout: (see sketch below)**



For every individual finger, the active diffusion area and side wall perimeter (excluding side adjacent to gate) for drain or source:

$M=\#\text{ of devices in parallel}=4$

And edge fingers side-wall perimeter, and inner fingers side wall perimeter respectively

$P_{\text{single\_edge}}=2\,x\,4\,\lambda+8\,\lambda=16\,\lambda=2.88\,\mu m$ $P_{\text{single\_inner}}=2\,x\,4\,\lambda=1.44\,\mu m$

Therefore for each NMOS transistor the total drain active diffusion area:

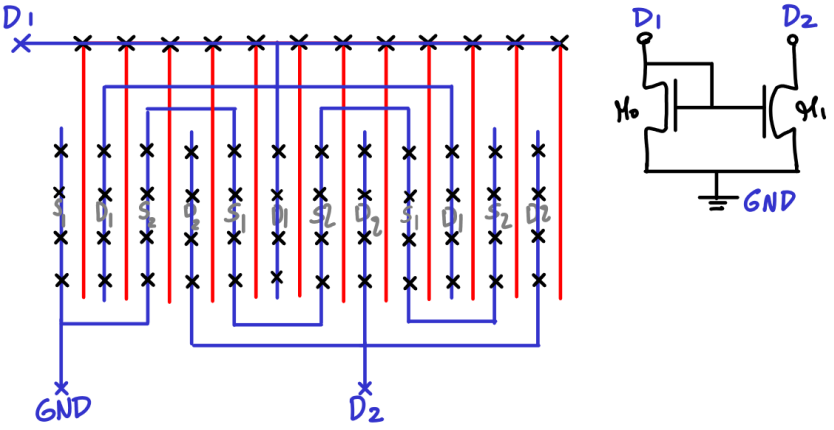
$A_d = 3\,x\,A_{single} = 3\,x\,5.76\,\mu m^2 = 17.28\,\mu m^2$

and the total source active diffusion area: $A_d = 3\,x\,A_{single} = 17.28\,\mu m^2$

And the total side-wall perimeter for drain (recalling to include only up and down sides for inner fingers; i.e. omitting to include sides adjacent to channel)

$P_d = 2\,x\,P_{single\_inner} + P_{single\_edge} = 2.88\,\mu m + 2.88\,\mu m = 5.76\,\mu m$ **and the total side-wall perimeter for source** $P_s = 2\,x\,P_{single\_inner} + P_{single\_edge} = 5.76\,\mu m$

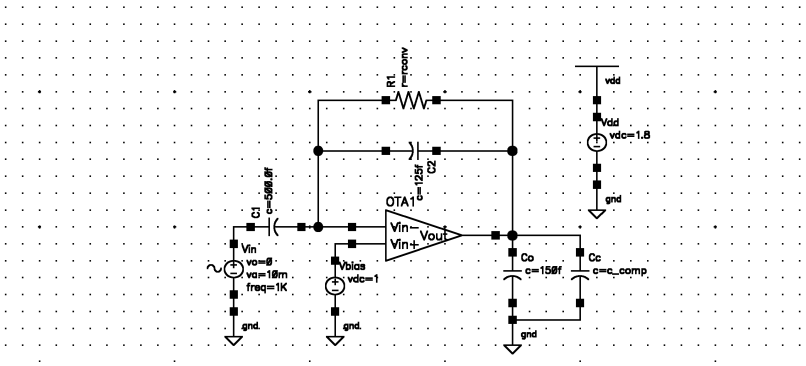
Furthermore, **a potential better layout to enhance matching between both transistors** and thus current matching in the mirror, is the following common-centroid standard technique (see sticks diagram below):

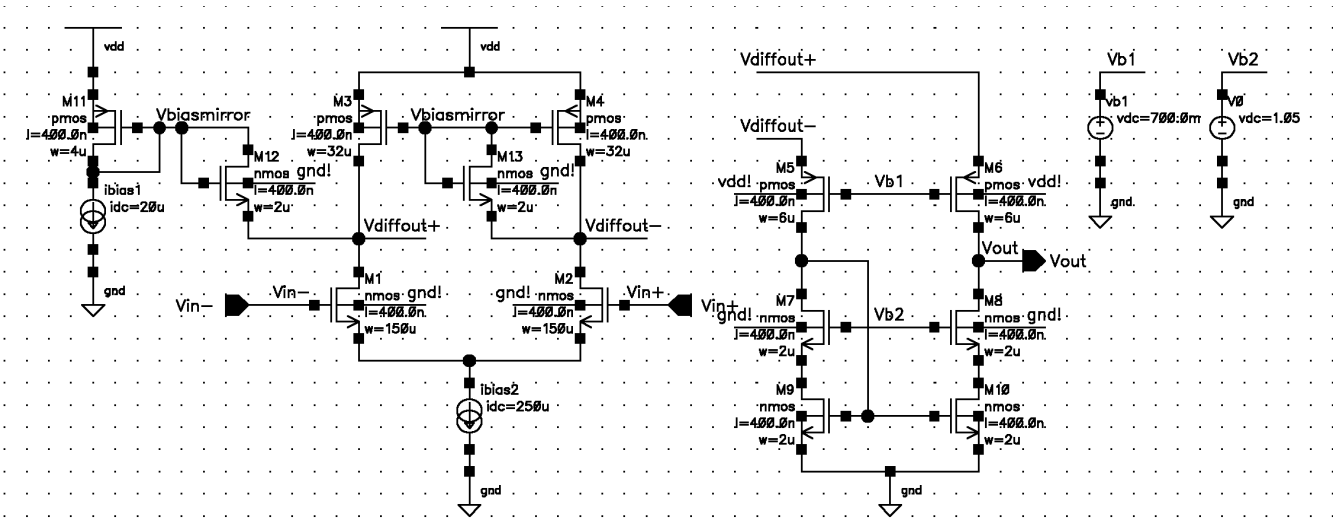


Part 2

Given the single-stage folded cascode opamp in the netlist and the closed loop inverting capacitive feedback configuration driving a capacitive load, we are asked to perform dominant pole compensation by selecting the compensation capacitor Cc to provide 80° phase margin.

Initially I draw the circuit by hand to put together the overall schematic (also referring to the textbook section on folded-cascode opamps). Then I entered the schematic to Cadence with all the device sizes and parameters from the netlist. (**see schematic of closed loop testbench and folded cascode OTA with device sizes and dc bias sources respectively**)

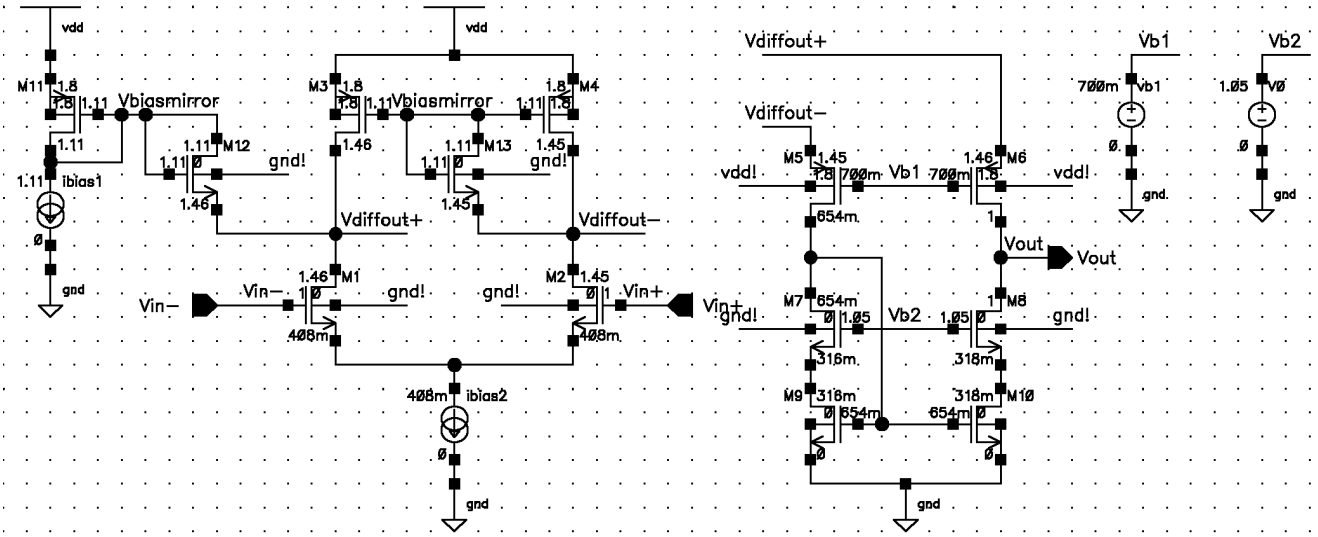




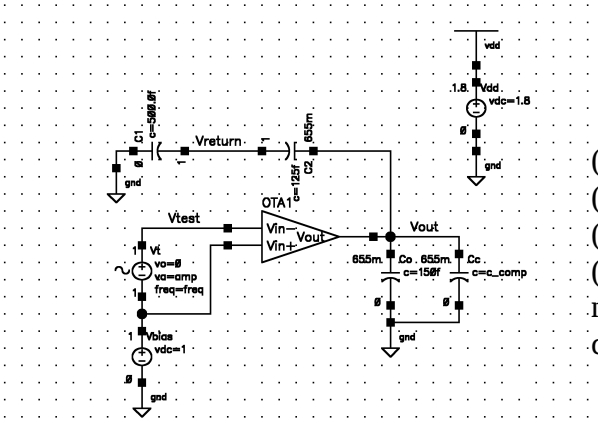
Now, first of all, we needed to make sure that the operating point of all transistors (no AC input signal applied) for the OTA all are in the saturation region except for the slew-rate clamp helpers M12 and M13 which should be in cutoff. (**see the formatted SPICE results to verify operating region of all transistors at DC, additionally see OTA node voltages on the next page**)

element	**1:m6**	**1:m5**	**1:m4**	**1:m3**	**1:m11**	**1:m10**	**1:m9**	**1:m8**	**1:m7**	**1:m13**	**1:m1**	**1:m12**
model	0:pmos	0:pmos	0:pmos	0:pmos	0:pmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos	0:nmos
region	**Saturati**	**Saturati**	**Saturati**	**Saturati**	**Saturati**	**Saturati**	**Saturati**	**Saturati**	**Saturati**	**Cutoff**	**Saturati**	**Cutoff**
id	-2.307e-05	-2.305e-05	-1.482e-04	-1.479e-04	-2.000e-05	2.307e-05	2.305e-05	2.307e-05	2.305e-05	-5.946e-16	1.249e-04	-5.951e-16
ibs	0.	0.	0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
ibd	0.	0.	0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
vgs	**-7.613e-01**	**-7.545e-01**	**-6.881e-01**	**-6.881e-01**	**-6.881e-01**	**6.541e-01**	**6.541e-01**	**7.316e-01**	**7.336e-01**	**-3.426e-01**	**5.921e-01**	**-3.494e-01**
vds	**-4.614e-01**	**-8.004e-01**	**-3.455e-01**	**-3.387e-01**	**-6.881e-01**	**3.184e-01**	**3.164e-01**	**6.814e-01**	**3.377e-01**	**-3.426e-01**	**1.053e+00**	**-3.494e-01**
vbs	3.387e-01	3.455e-01	0.	0.	0.	0.	0.	-3.184e-01	-3.164e-01	-1.454e+00	-4.078e-01	-1.461e+00
vth	**-5.530e-01**	**-5.535e-01**	**-4.560e-01**	**-4.560e-01**	**-4.524e-01**	**4.592e-01**	**4.592e-01**	**5.491e-01**	**5.486e-01**	**7.254e-01**	**5.735e-01**	**7.254e-01**
vdsat	**-1.890e-01**	**-1.837e-01**	**-2.002e-01**	**-2.002e-01**	**-1.991e-01**	**1.540e-01**	**1.540e-01**	**1.567e-01**	**1.583e-01**	**4.222e-02**	**6.097e-02**	**4.222e-02**
vod	-2.083e-01	-2.010e-01	-2.322e-01	-2.321e-01	-2.357e-01	1.949e-01	1.948e-01	1.825e-01	1.849e-01	-1.068e+00	1.854e-02	-1.074e+00
beta	1.124e-03	1.126e-03	6.308e-03	6.308e-03	7.877e-04	1.590e-03	1.590e-03	1.606e-03	1.606e-03	1.625e-03	1.190e-01	1.625e-03
gam eff	4.688e-01	4.686e-01	4.835e-01	4.835e-01	4.794e-01	5.748e-01	5.748e-01	5.732e-01	5.732e-01	5.700e-01	5.747e-01	5.700e-01
gm	**1.976e-04**	**2.018e-04**	**1.163e-03**	**1.161e-03**	**1.537e-04**	**2.324e-04**	**2.322e-04**	**2.398e-04**	**2.359e-04**	**1.816e-14**	**2.793e-03**	**1.817e-14**
gds	5.383e-06	4.860e-06	4.072e-05	4.150e-05	4.130e-06	5.381e-06	5.432e-06	1.118e-06	3.253e-06	8.327e-17	9.479e-06	8.247e-17
gmb	5.484e-05	5.591e-05	3.658e-04	3.650e-04	4.744e-05	2.352e-04	2.339e-04	5.535e-05	5.449e-05	4.128e-15	6.540e-04	4.132e-15
cdtot	4.115e-15	4.101e-15	2.219e-14	2.221e-14	2.735e-15	1.380e-15	1.381e-15	1.380e-15	1.392e-15	1.379e-15	1.047e-13	1.379e-15
cgtot	2.250e-14	2.247e-14	1.210e-13	1.210e-13	1.510e-14	7.795e-15	7.795e-15	7.701e-15	7.717e-15	3.972e-15	4.817e-13	3.972e-15
cstot	1.140e-14	1.138e-14	6.227e-14	6.227e-14	7.737e-15	5.491e-15	5.482e-15	3.867e-15	3.873e-15	1.389e-15	2.245e-13	1.389e-15
cbtot	3.498e-15	3.487e-15	2.181e-14	2.182e-14	2.708e-15	8.054e-16	8.105e-16	1.343e-15	1.347e-15	1.216e-15	9.894e-14	1.216e-15
cgs	1.805e-14	1.802e-14	9.666e-14	9.666e-14	1.205e-14	9.854e-15	9.830e-15	5.986e-15	5.993e-15	1.389e-15	3.260e-13	1.389e-15
cgd	4.082e-15	4.069e-15	2.204e-14	2.206e-14	2.715e-15	1.356e-15	1.357e-15	1.380e-15	1.392e-15	1.367e-15	1.047e-13	1.367e-15

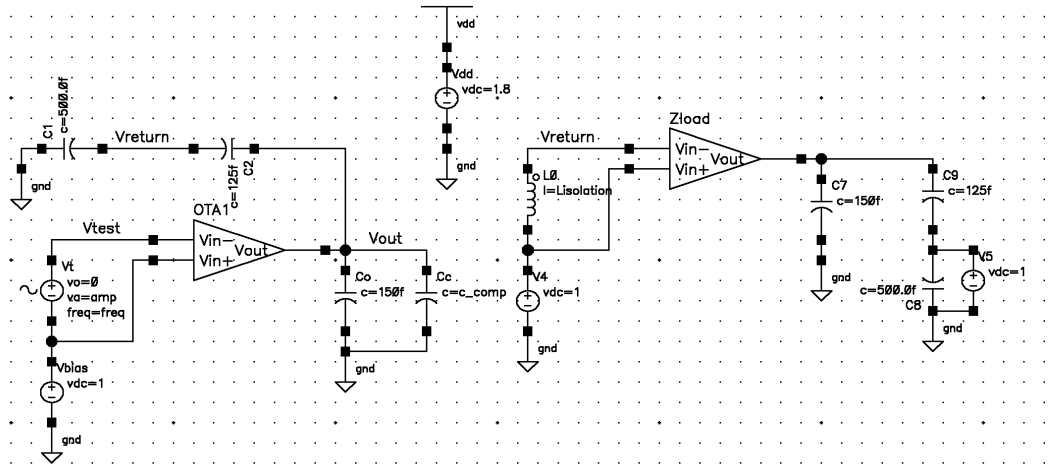
element	**1:m2**
model	0:nmos
region	**Saturati**
id	1.251e-04
ibs	0.
ibd	0.
vgs	**5.922e-01**
vds	**1.046e+00**
vbs	-4.078e-01
vth	**5.735e-01**
vdsat	**6.102e-02**
vod	1.867e-02
beta	1.190e-01
gam eff	5.747e-01
gm	**2.798e-03**
gds	9.503e-06
gmb	6.553e-04
cdtot	1.047e-13
cgtot	4.819e-13
cstot	2.247e-13
cbtot	9.894e-14
cgs	3.263e-13
cgd	1.047e-13



Now we need to simulate the **open loop response of the circuit** in order to arrive at our current transition frequency Ft and phase margin. To break the loop, it is convenient and recommended to break the loop such that the input impedance where the test source would be applied is very high (ideally infinite). In this case it is often appropriate to break the loop at the opamp inputs (high impedance looking in: Zin), and then make sure to provide a test load at the return path that is equivalent to that input impedance. To provide a realistic test load one can copy the circuit under test (operating under the same bias and operating points) and use it as the test load Ztest to be applied to the Vreturn output (sometimes called self-loading), more precisely graphically:

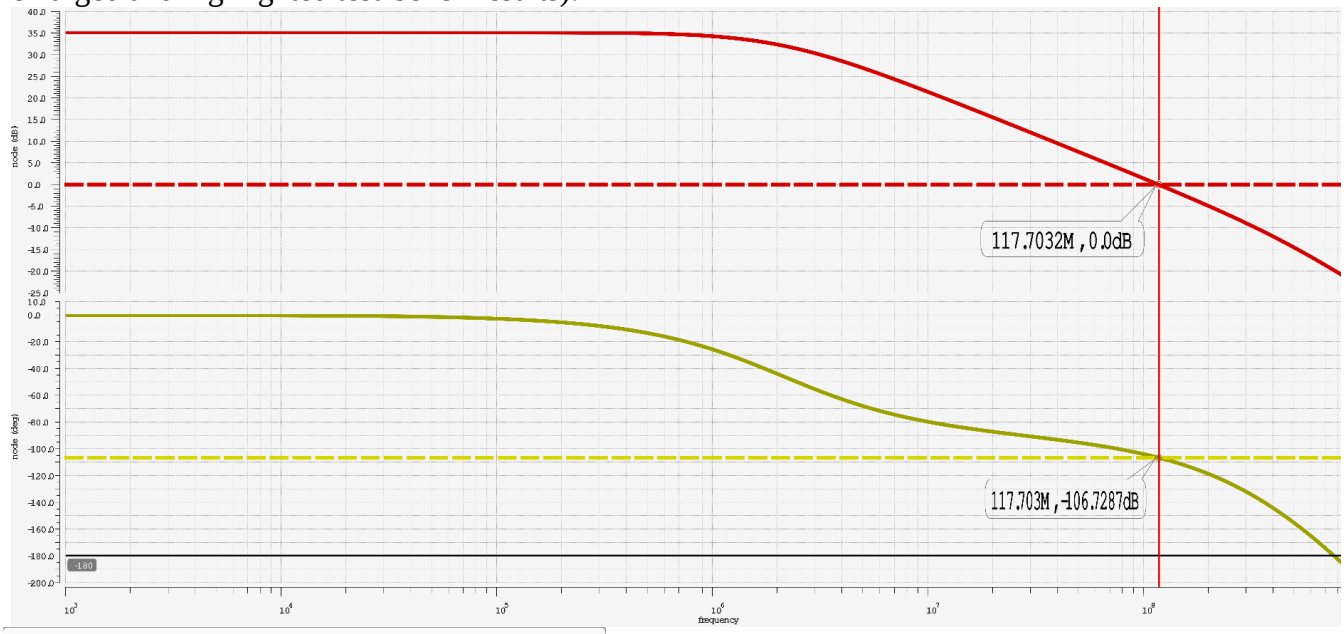


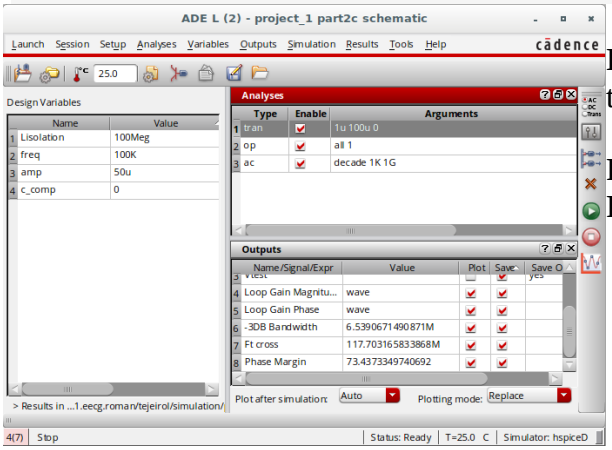
(1) Break the loop
(2) Apply a test input Vtest
(3) monitor returned voltage Vreturn
(4) Apply a realistic Ztest load (below)
note: very large isolation inductor is used to establish common bias points at DC.



Starting from the uncompensated (Cc=0) to understand, there are a couple of interesting things worth noting, simulating the uncompensated open loop response unloaded (I.e. assuming the simple case of an ideal opamp infinite input impedance) leads to a much larger unity gain transition frequency (in comparison with the loaded open loop response) as should be expected given the finite input impedance of the diff pair: Hence it makes sense to use a realistic test load to calculate the open loop response in this case.

The starting uncompensated open-loop response of the circuit is (see bode plot below, with text enlarged and highlighted test-bench results):

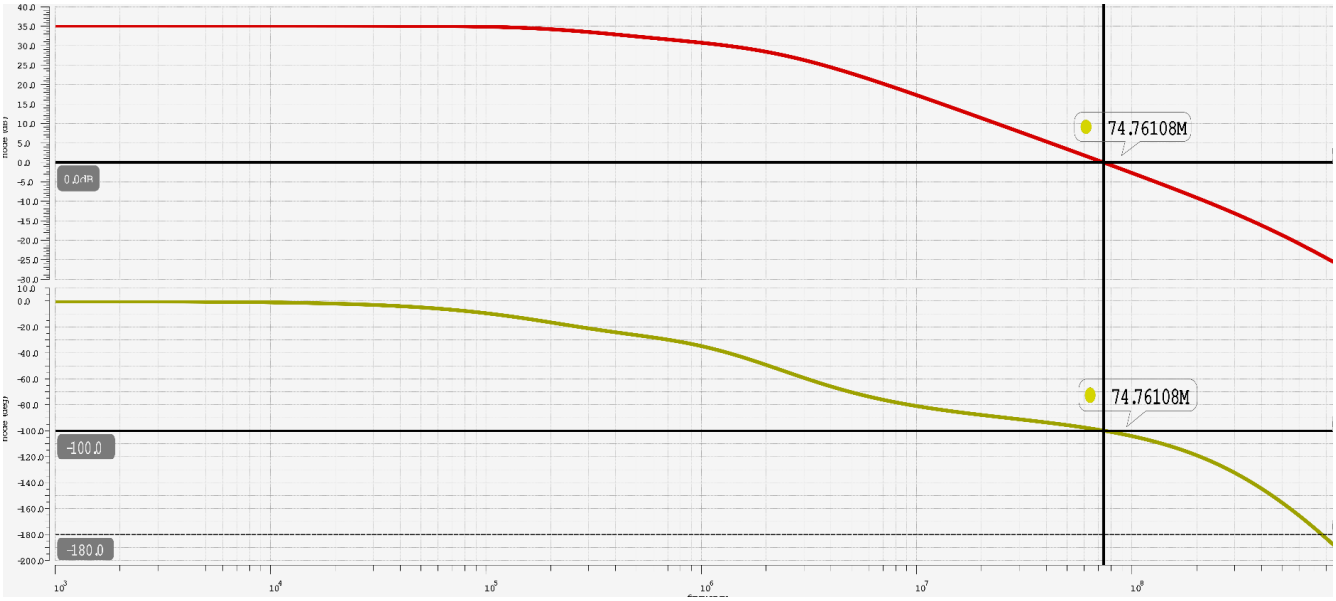


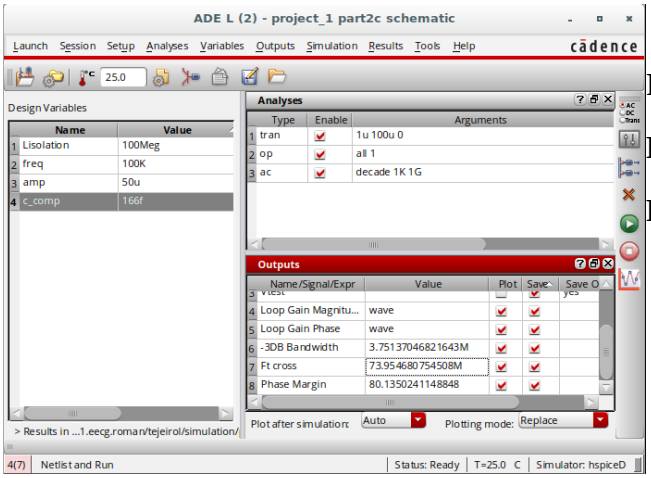


Here it can be seen that for the uncompensated case the transition frequency and phase margin are:

Ft = 117.703MHz
PM = 73.437 degrees

To compensate our folded-cascode opamp using dominant pole compensation, in order to bring our first pole to a lower frequency and arrive at our desired phase margin of 80 degrees, we can add a compensation capacitor at the output. In fact, from our uncompensated bode-plot we can see the lower transition frequency that is needed in order to increase the phase margin to 80 degrees. As we increase the value of our compensation capacitor parametrically we can see the open-loop magnitude response shift back (decreasing bandwidth) until we can arrive at our **compensation capacitor desired value of 166fF, giving us a phase margin of 80.135 degrees** (**see the bode-plot with markers text enlarged, and highlighted testbench results below**)



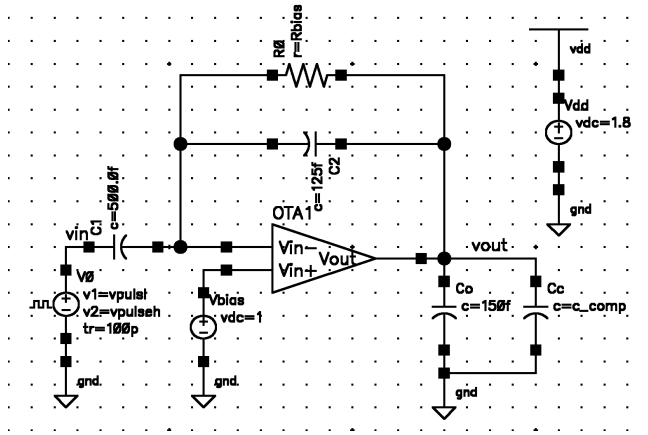


For a dominant pole compensation with **Cc = 166fF**

Ft = 73.955MHz

Phase Margin = 80.135 degrees

Finally to measure the slew rate, we go back to our closed-loop testbench but apply a large pulse to the input of the amplifier (such that the opamp is slewing: one of the diff-pairs is in cutoff, and all current flows through one branch only), graphically:



Where our pulse source:

Vpulse_high = 1.25V

Vpulse_low = 750mV

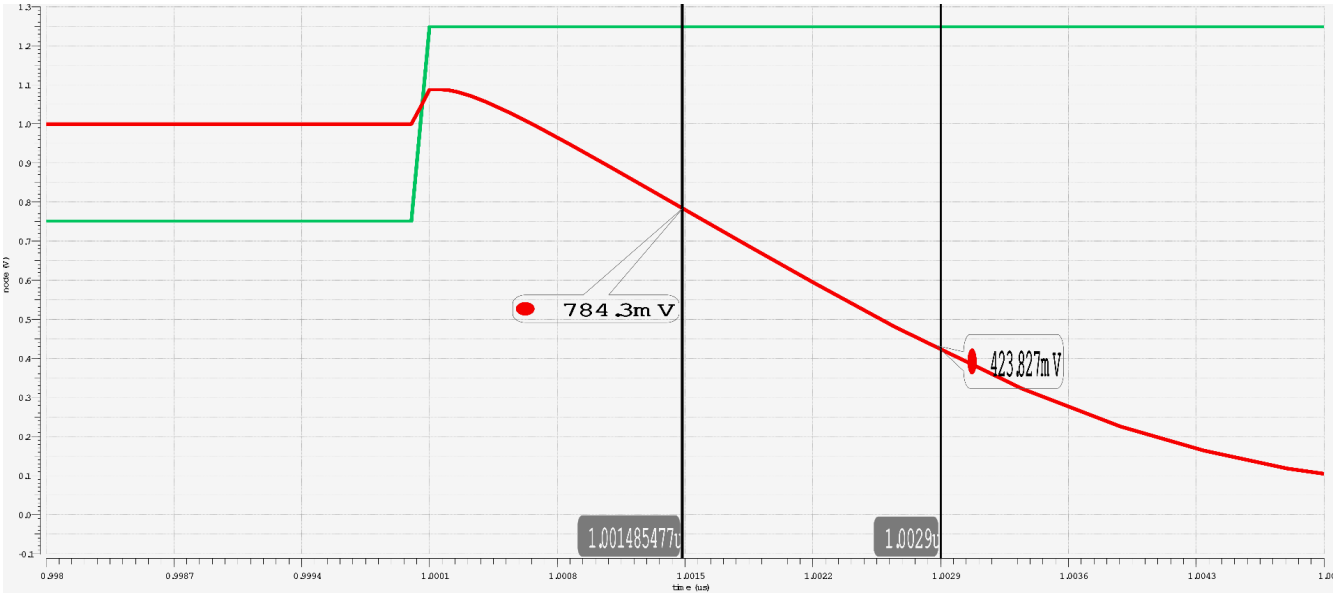
Trise = 100pS

Tfall = 100ps

Period = 1µS

Pulse_width = 0.5µS

Then, from the transient response, we look at the time window where the opamp is slewing – where the output voltage is increasing linearly – and measure the slope to define the slew rate for the opamp:

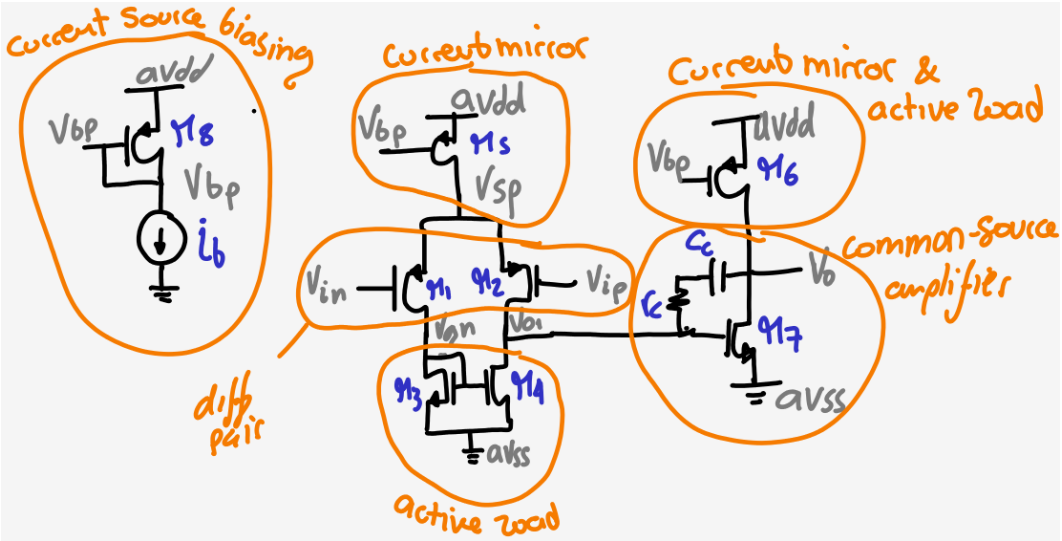


The slew rate for the opamp is (note this is an inverting feedback configuration as mentioned before):

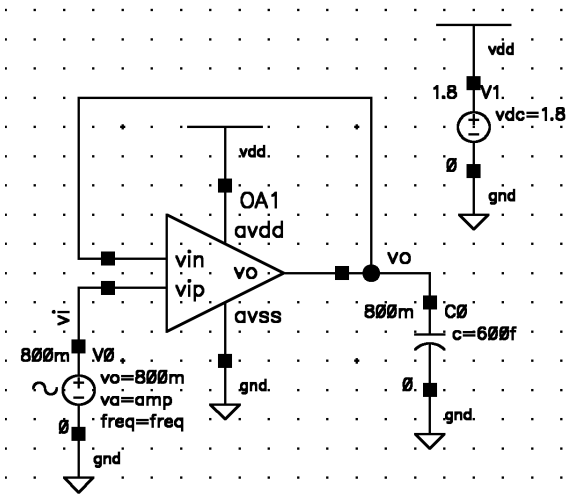
$$Slew\ Rate = \frac{\Delta Vout}{\Delta time} = \frac{423.827\,mV - 784.3\,mV}{1.0029\,\mu S - 1.0014\,\mu s} = -253.85\,\frac{V}{\mu S}$$

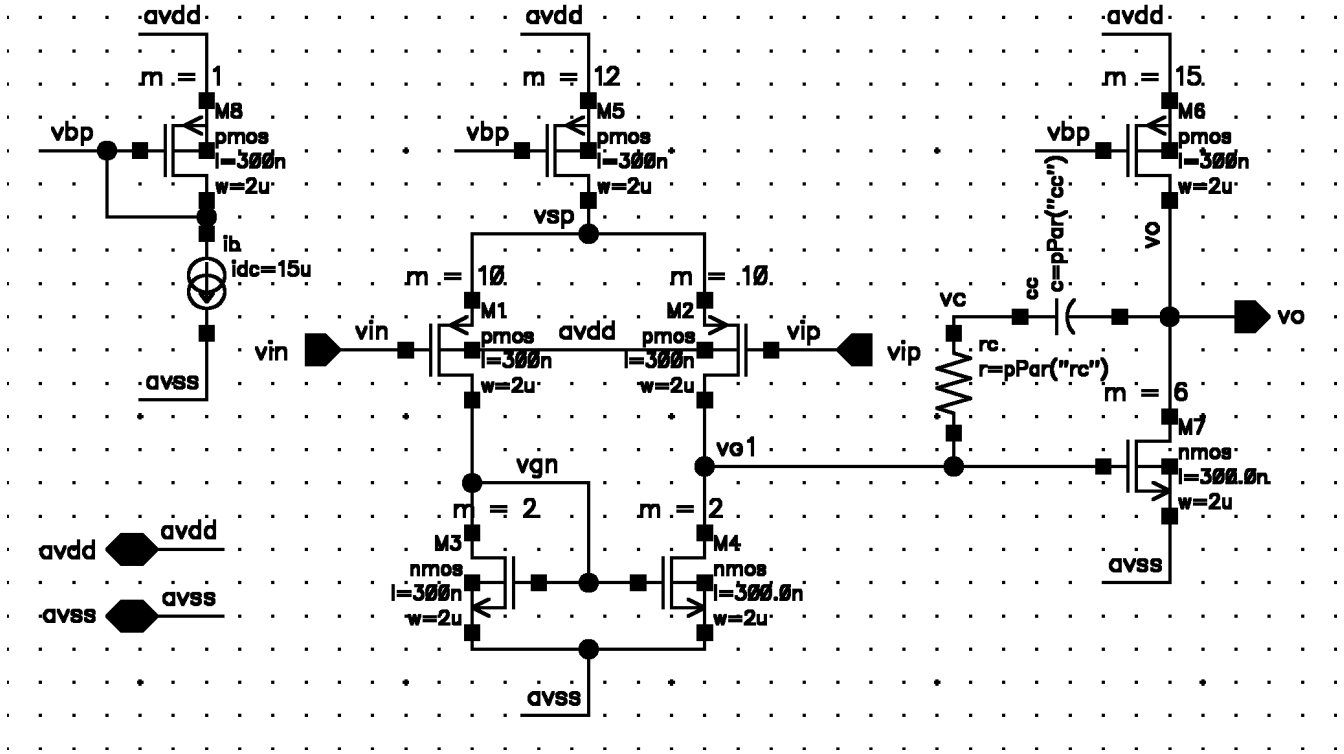
Part 3

For part 3 of the assignment we are provided the netlist for a 2-stage opamp design, the opamp is meant to be in a unity gain configuration driving a capacity load. Once again we start by parsing the netlist by hand and drawing every circuit-block of the opamp on paper (in this case all transistors are based off on multipliers of a unit transistor of size W/L = 2µm/200nm ~ 6.667)



Subsequently we entered our schematic on Cadence with all transistors parameters. (see the schematic of the unity-gain closed-loop testbench and 2nd-stage opamp with device sizes and bias sources respectively)

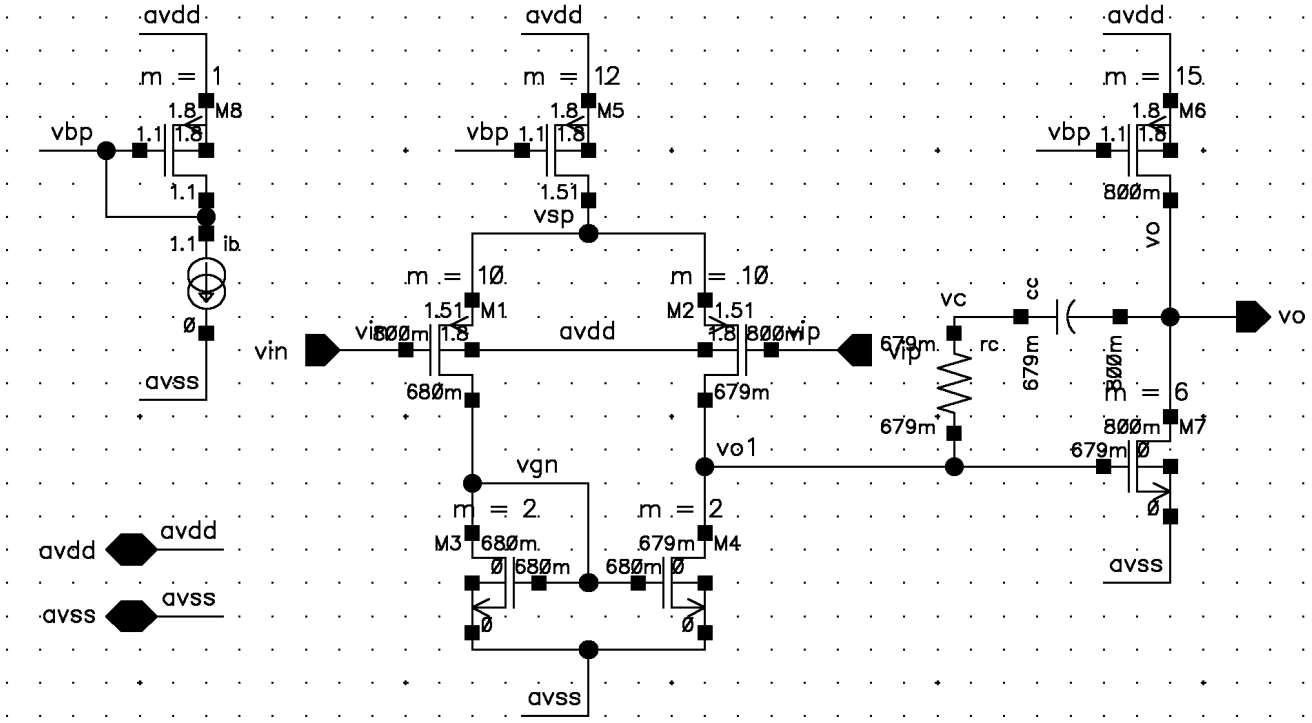




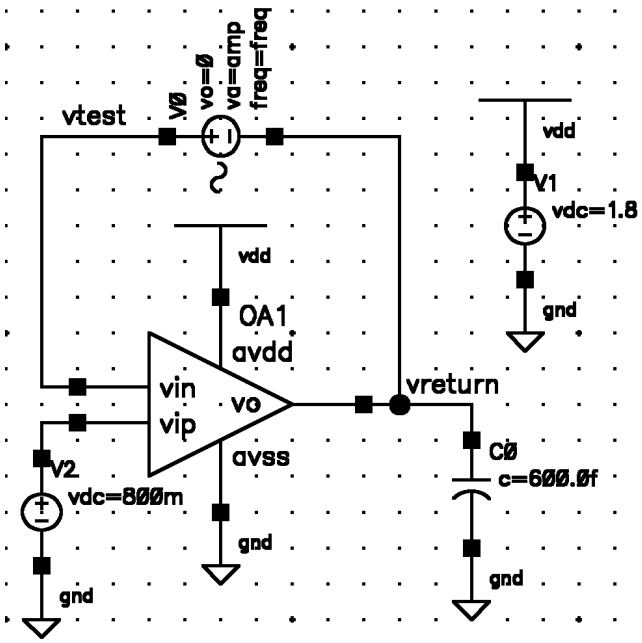
Now, we needed to make sure that the operating point of all transistors (no AC input signal applied) for the opamp all are in the saturation or active region. (**see formatted SPICE OP results**)

element	1:m7	1:m4	1:m3	1:m6	1:m8	1:m5	1:m2	1:m1
model	0:nmos	0:nmos	0:nmos	0:pmos	0:pmos	0:pmos	0:pmos	0:pmos
region	**Saturati**	**Saturati**	**Saturati**	**Saturati**	**Saturati**	**Saturati**	**Saturati**	**Saturati**
id	2.413e-04	7.988e-05	7.990e-05	-2.413e-04	-1.500e-05	-1.598e-04	-7.988e-05	-7.990e-05
ibs	0.	0.	0.	0.	0.	0.	0.	0.
ibd	0.	0.	0.	0.	0.	0.	0.	0.
vgs	**6.786e-01**	**6.799e-01**	**6.799e-01**	**-7.016e-01**	**-7.016e-01**	**-7.016e-01**	**-7.095e-01**	**-7.096e-01**
vds	**7.999e-01**	**6.786e-01**	**6.799e-01**	**-1.000e+00**	**-7.016e-01**	**-2.905e-01**	**-8.309e-01**	**-8.296e-01**
vbs	0.	0.	0.	0.	0.	0.	2.905e-01	2.905e-01
vth	**4.671e-01**	**4.681e-01**	**4.681e-01**	**-4.603e-01**	**-4.614e-01**	**-4.630e-01**	**-5.447e-01**	**-5.447e-01**
vdsat	**1.639e-01**	**1.640e-01**	**1.640e-01**	**-2.029e-01**	**-2.021e-01**	**-2.010e-01**	**-1.548e-01**	**-1.549e-01**
vod	2.116e-01	2.118e-01	2.118e-01	-2.413e-01	-2.402e-01	-2.386e-01	-1.648e-01	-1.649e-01
beta	1.339e-02	4.464e-03	4.464e-03	8.285e-03	5.522e-04	6.624e-03	5.359e-03	5.359e-03
gam eff	5.742e-01	5.742e-01	5.742e-01	4.708e-01	4.708e-01	4.708e-01	4.588e-01	4.588e-01
gm	**2.177e-03**	**7.214e-04**	**7.214e-04**	**1.765e-03**	**1.118e-04**	**1.206e-03**	**8.259e-04**	**8.259e-04**
gds	3.554e-05	1.241e-05	1.240e-05	5.440e-05	3.691e-06	6.901e-05	2.191e-05	2.192e-05
gmb	4.917e-03	1.409e-03	1.411e-03	5.359e-04	3.388e-05	3.648e-04	2.257e-04	2.257e-04
cdtot	8.206e-15	2.736e-15	2.736e-15	2.047e-14	1.365e-15	1.664e-14	1.364e-14	1.364e-14
cgtot	3.842e-14	1.281e-14	1.281e-14	9.231e-14	6.155e-15	7.406e-14	6.103e-14	6.103e-14
cstot	3.679e-14	1.139e-14	1.139e-14	4.676e-14	3.119e-15	3.746e-14	3.058e-14	3.058e-14
cbtot	-2.383e-15	-3.321e-16	-3.369e-16	1.420e-14	9.465e-16	1.143e-14	8.315e-15	8.315e-15
cgs	7.237e-14	2.191e-14	2.193e-14	7.007e-14	4.673e-15	5.612e-14	4.640e-14	4.640e-14
cgd	8.095e-15	2.699e-15	2.699e-15	2.035e-14	1.357e-15	1.653e-14	1.356e-14	1.356e-14

And Opamp node voltages accordingly

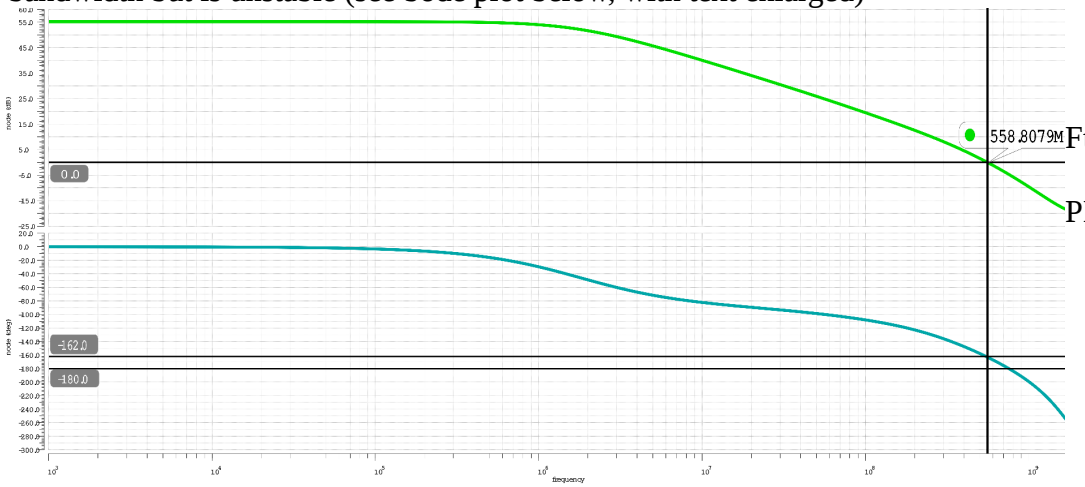


Subsequently, we need to break the loop in order to assess the current uncompensated open-loop response of the circuit: we need to know the starting unity gain frequency and phase margin. In this case, because we have a common unity gain configuration, to open the loop, we can employ the useful technique of inserting a purely AC source into the feedback loop (our test signal).



Because the DC value of this source is 0, the DC bias voltages for the circuit remain undisturbed, and furthermore the loading seen at the return path is that of both the capacitive load and input impedance of the Opamp itself as required.

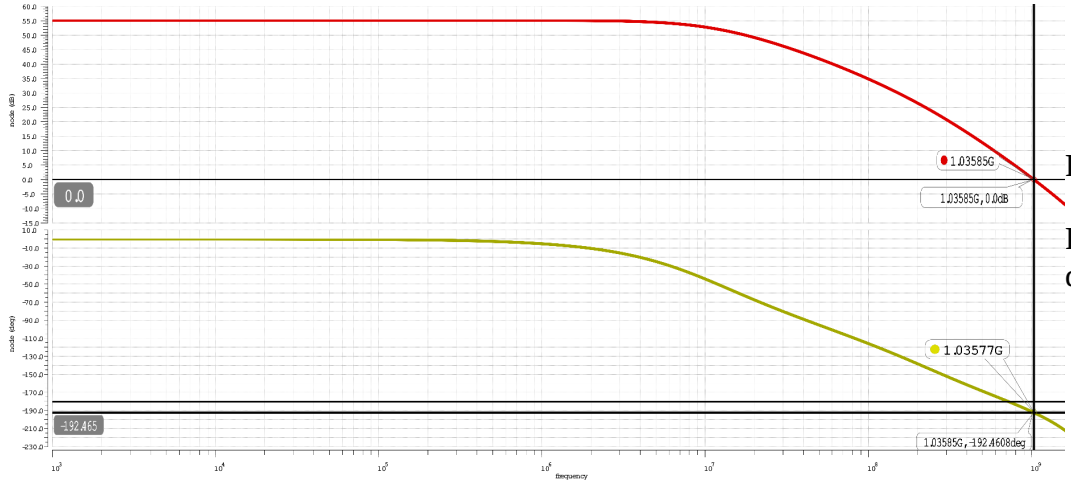
The open-loop response of the circuit with the default compensation values possesses a large bandwidth but is unstable (see bode plot below, with text enlarged)



Ft = 558.808MHz

PM = 18 degrees

Similarly, (for interest-sake) the uncompensated open-loop response of the circuit possesses an even larger bandwidth but is unstable as expected (positive feedback) (see bode plot below, with text enlarged and highlighted test-bench results)



Ft = 1.03585GHz

PM = -12.465 degrees

The compensation procedure in our case outlined in chapter 6 of our textbook (page 256). Initially we budgeted for dominant pole compensation to get us to a 55 degrees phase margin (following the procedure in the book) and subsequently allow for lead compensation to get us the extra 20 degrees needed to a phase margin of 75 degrees. The systematic compensation steps followed:

1. Start by choosing a starting point for $Cc' = \frac{\beta\, gm_1}{gm_7} C_l$

For a unity gain feedback configuration our feedback factor β=1. Cl = 0.6pF from our given specifications and from our SPICE simulation our transistor transconductances gm1 = 0.8259mS and gm7 = 2.177mS.

Therefore $Cc' = \frac{0.8259\, mS}{2.177\, mS} 0.6\, pF = 1.5815\, pF$

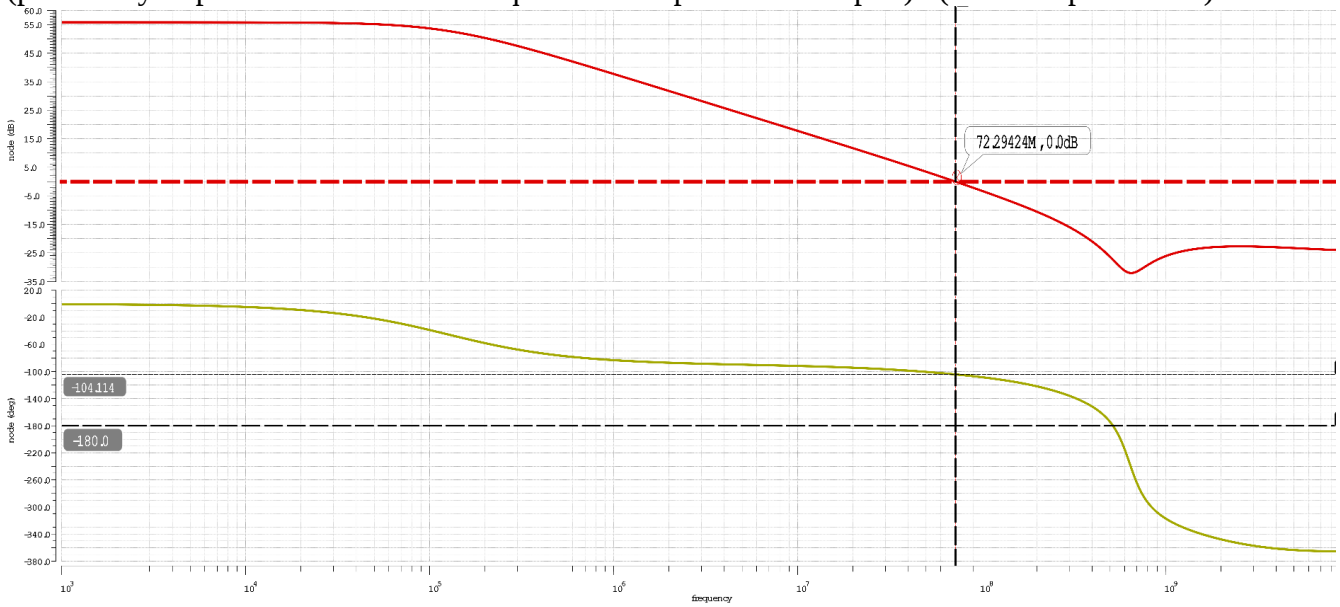
2. Find the frequency (Ft) and gain (A') where a phase shift of -125 degrees occurs.
From our SPICE simulation plot we get: Ft = 87.6582MHz and A' = -1.3504dB or 0.85601 V/V

3. Choose and modify Cc such that Ft becomes our new transition frequency, resulting in a dominant pole compensation leading to 55 degrees phase margin.
We can calculate our desired Cc to be $Cc = Cc'A' = 1.5815\,pF\,x\,0.85601 = 1.3538\,pF$ which is indeed very close to our optimal value of 1.3348pF from our SPICE simulation leading to 55 degrees phase margin.

4. Now choose our starting Rc according to $Rc = \frac{1}{2.7\,w_t C_c} = \frac{1}{2.7\,x\,2\pi\,x\,1.3538\,pF} = 496.717\,\Omega$

Note we needed to modify the given equation slightly as we want an additional phase margin of 20 degrees instead of 30 given in the book. Therefore we need a factor of 2.7 in the denominator
$atan(1/2.7) \sim 20\,degrees$

From our compensation procedure, we indeed arrive at a phase margin of PM=75.88 degrees with a good phase response at Ft=72.29MHz, however in the magnitude response, there is a sharp dip in the magnitude response past Ft and subsequently the slope does not continue to decrease at -20dB/dec as expected given the remaining dominant pole, this would lead to problems in the transient response (potentially imperfect cancellation of equivalent 2nd pole and zero pair) . (see bode plot below)

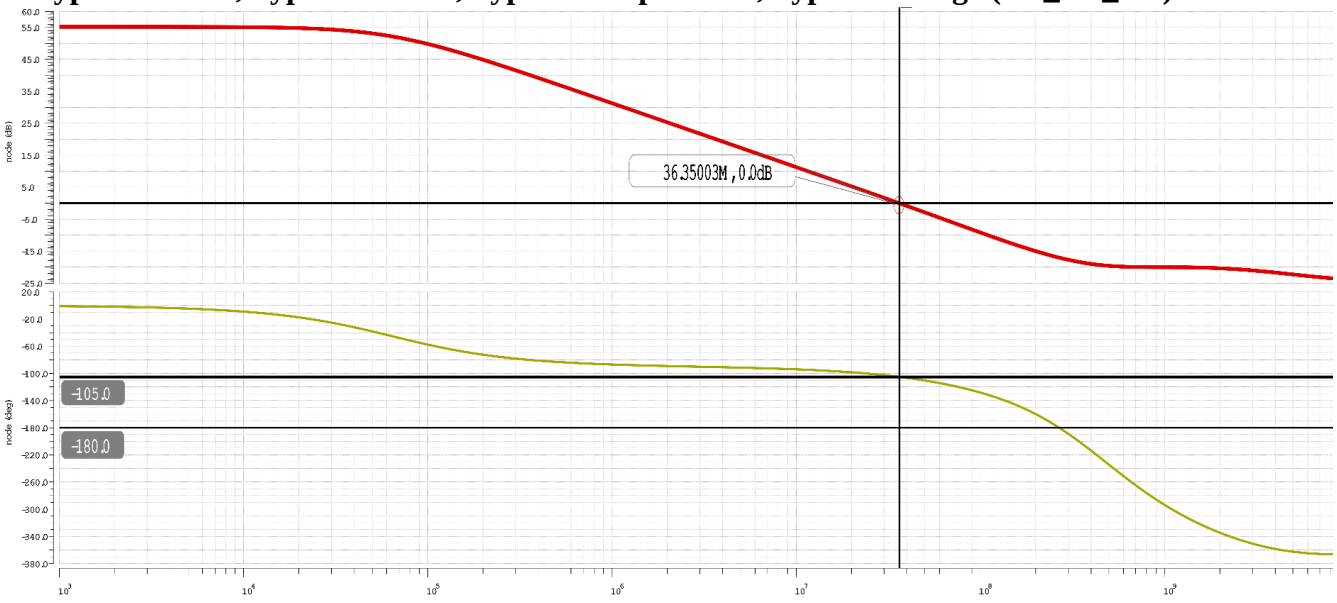


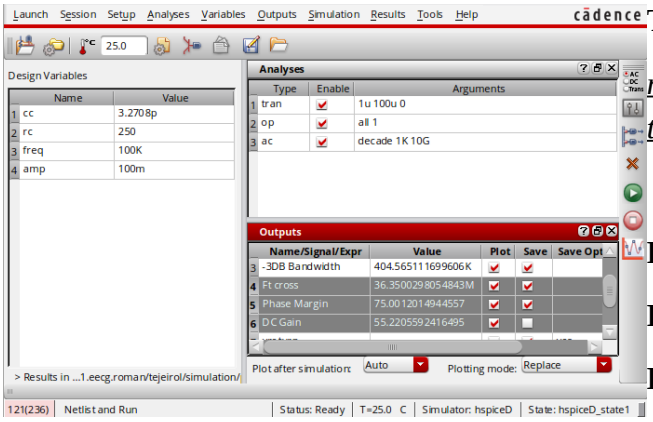
To help find a solution for this issue, we chose to set a more conservative target for lead compensation of 10 degrees, and modify dominant pole compensation to give us a starting phase margin of PM = 65 degrees (by increasing the compensation capacitor to an approximate value).

Subsequently we used a parametric analysis around Cp and sweeping Rc to find optimal combinations that would allow for our expected magnitude response (-40db/dec, flat upon pole zero cancellation, continuing on to -20dB/dec); as it turns out enforcing PM=75 degrees and optimizing for the values of Rc and Cc: it is interesting to note that Rc values above ~350Ω (with their respective Cc values) all lead to peaking/dip in the magnitude response. Therefore, in our case we settled for adequate **compensation values of Cp = 3.2708pF and Rc = 250Ω leading to our typical response** (**TT_TT_TT_TV**, see below).

All other corner responses were simulated by changing the included SPICE model card, simulation temperature and DC source parameters. For the SF_HT_LV and FS_HT_LV corners we put together Slow-PMOS/Fast-NMOS and Fast-PMOS/Slow-NMOS model cards to included for these corners.

1. Typical PMOS, Typical NMOS, Typical Temperature, Typical Voltage (TT_TT_TV) Corner





Testbench Results

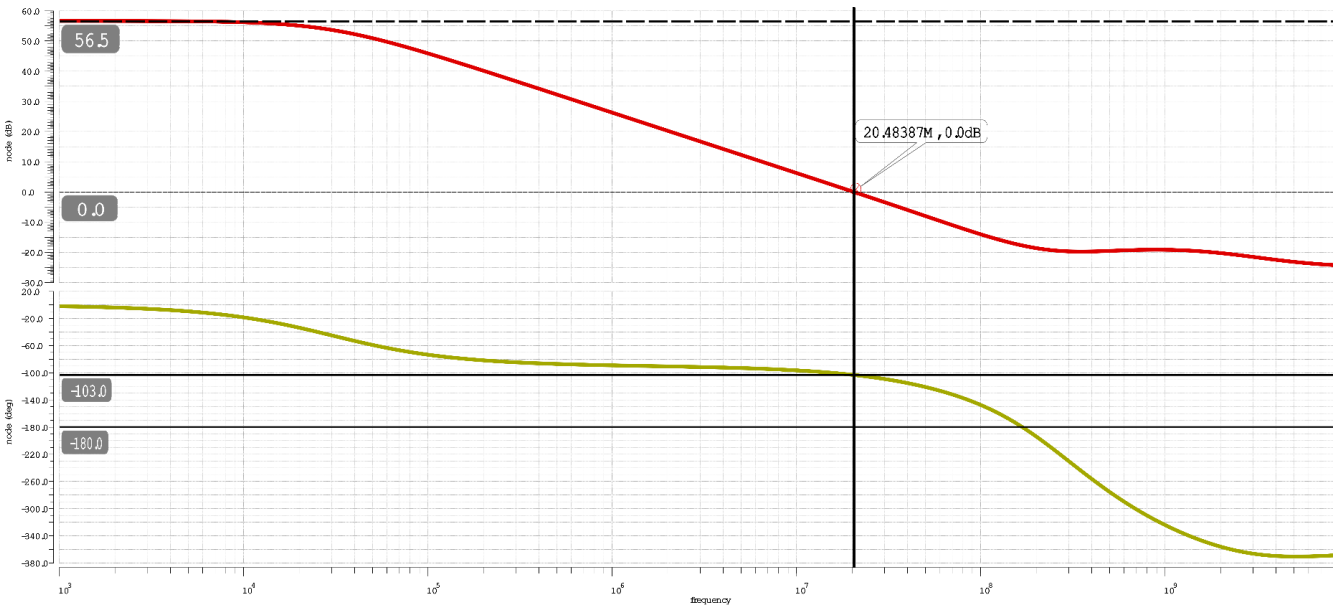
note testbench (calculator) results are more accurate than hand-placed plot markers

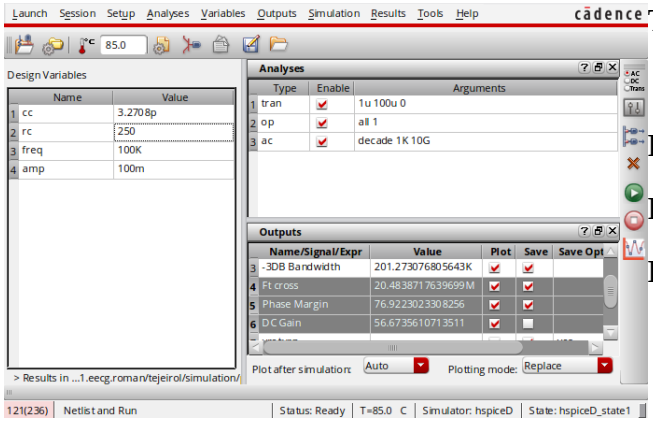
Ft = 36.35MHz

Phase Margin = 75 Degrees

DC Gain = 55.221 dB

2. Slow PMOS, Slow NMOS, High Temperature, Low Voltage (SS_HT_LV) Corner





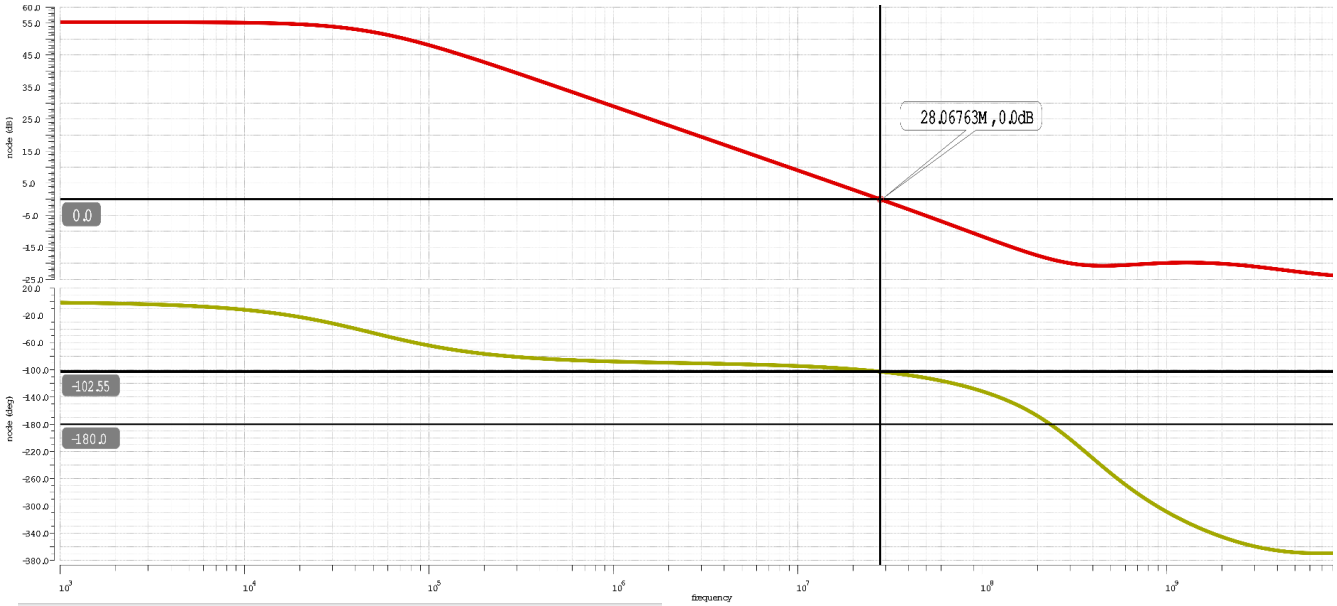
Testbench Results

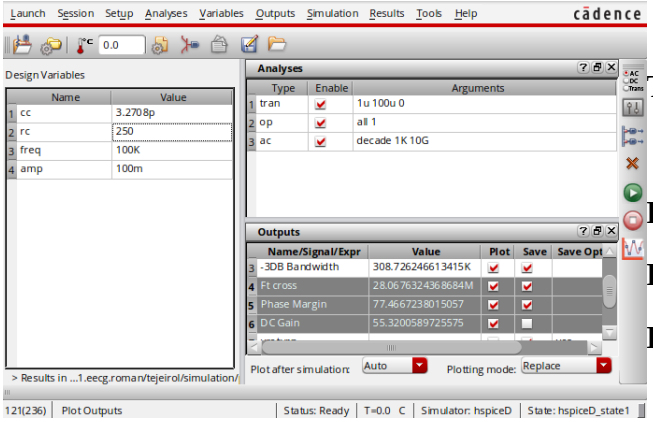
Ft = 20.484MHz

Phase Margin = 76.922 Degrees

DC Gain = 56.674 dB

3. Slow PMOS, Slow NMOS, Low Temperature, Low Voltage (SS_LT_LV) Corner





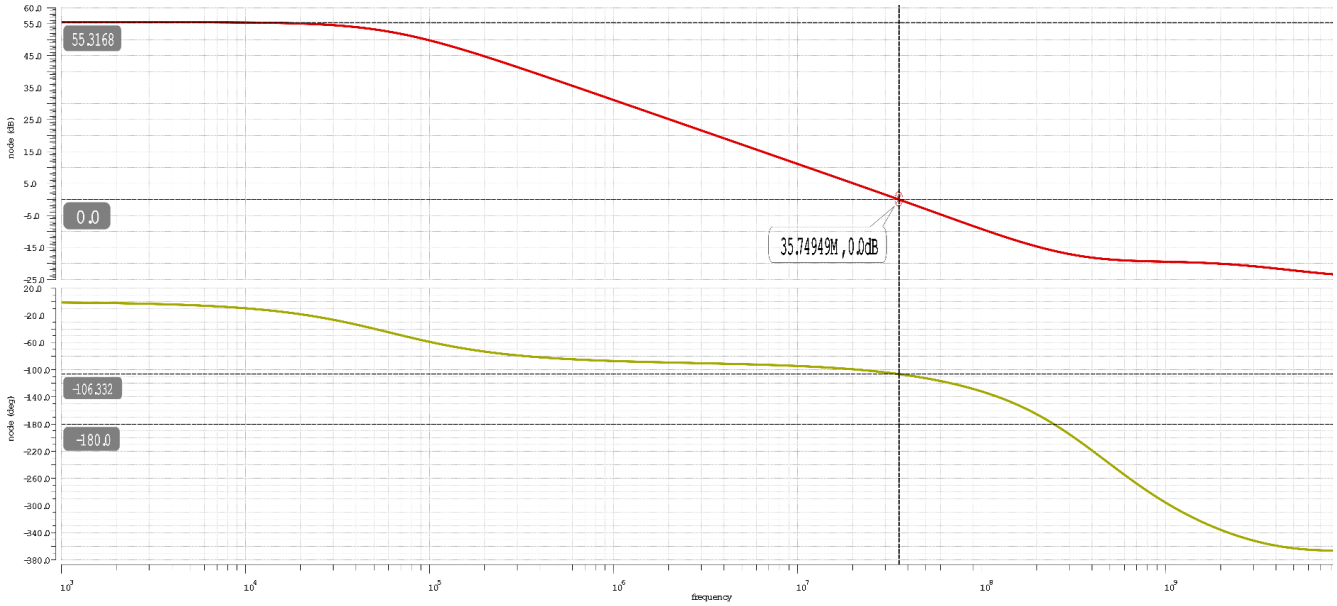
Testbench Results

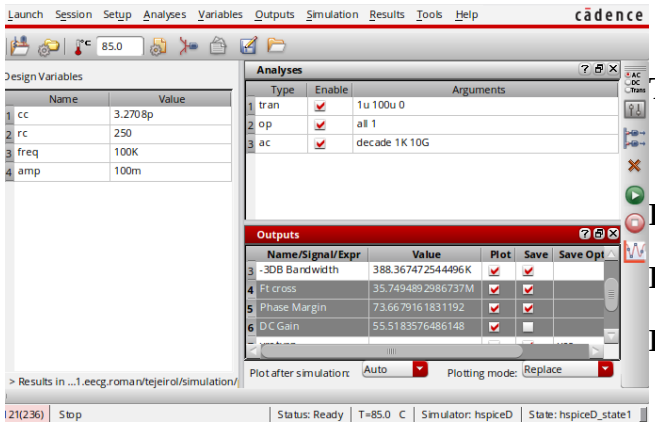
Ft = 28.068 MHz

Phase Margin = 77.467 Degrees

DC Gain = 55.320 dB

4. Fast PMOS, Fast NMOS, High Temperature, High Voltage (FF_HT_HV) Corner





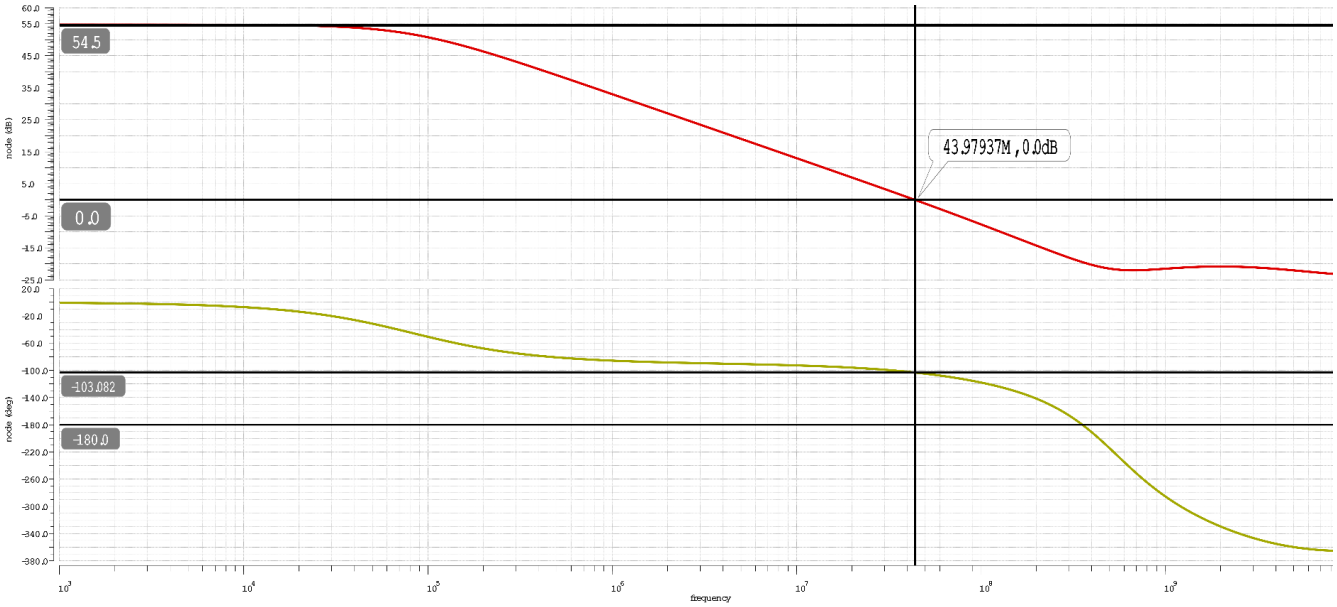
Testbench Results

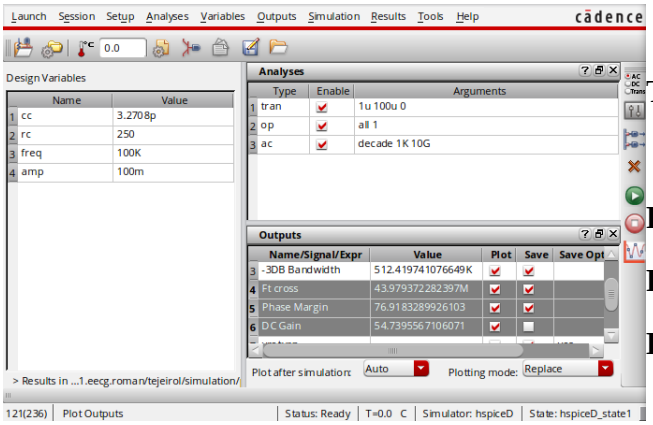
Ft = 35.749 MHz

Phase Margin = 73.668 Degrees

DC Gain = 55.518 dB

5. Fast PMOS, Fast NMOS, Low Temperature, High Voltage (FF_LT_HV) Corner





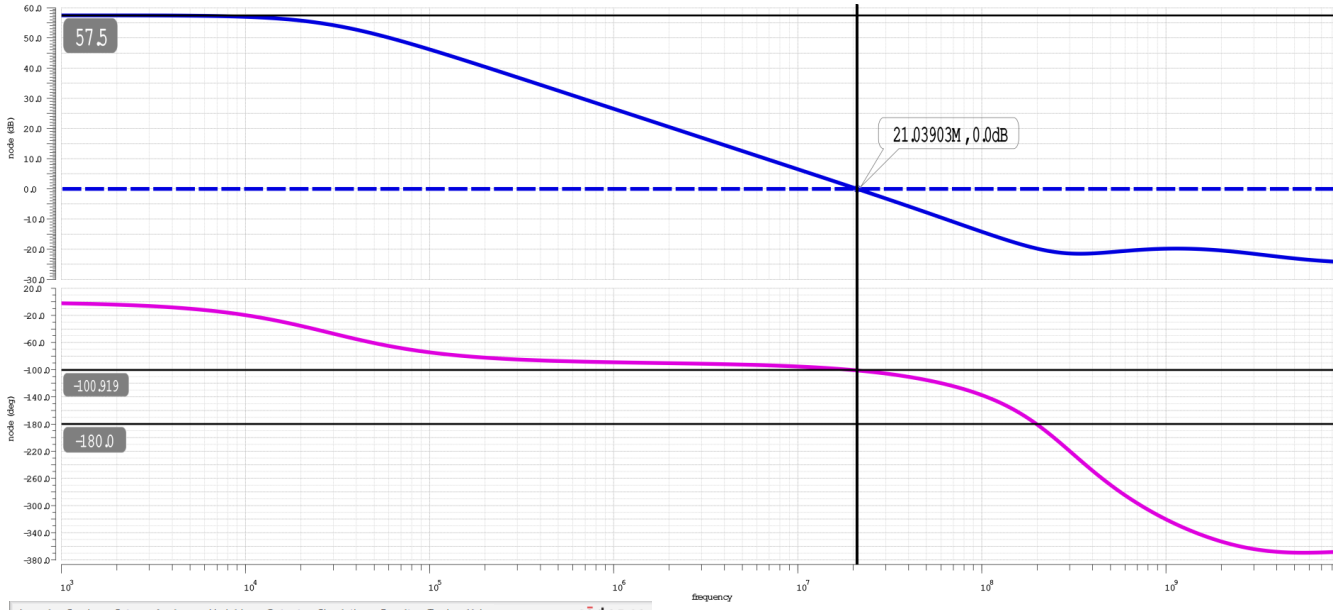
Testbench Results

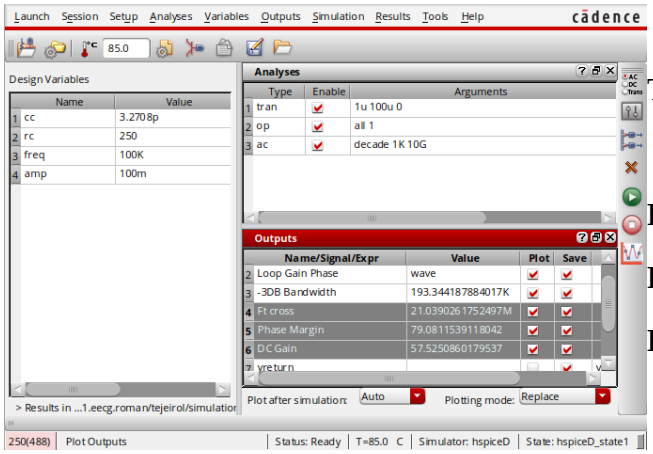
Ft = 43.979 MHz

Phase Margin = 76.918 Degrees

DC Gain = 54.74 dB

6. Slow PMOS, Fast NMOS, High Temperature, Low Voltage (SF_HT_LV) Corner





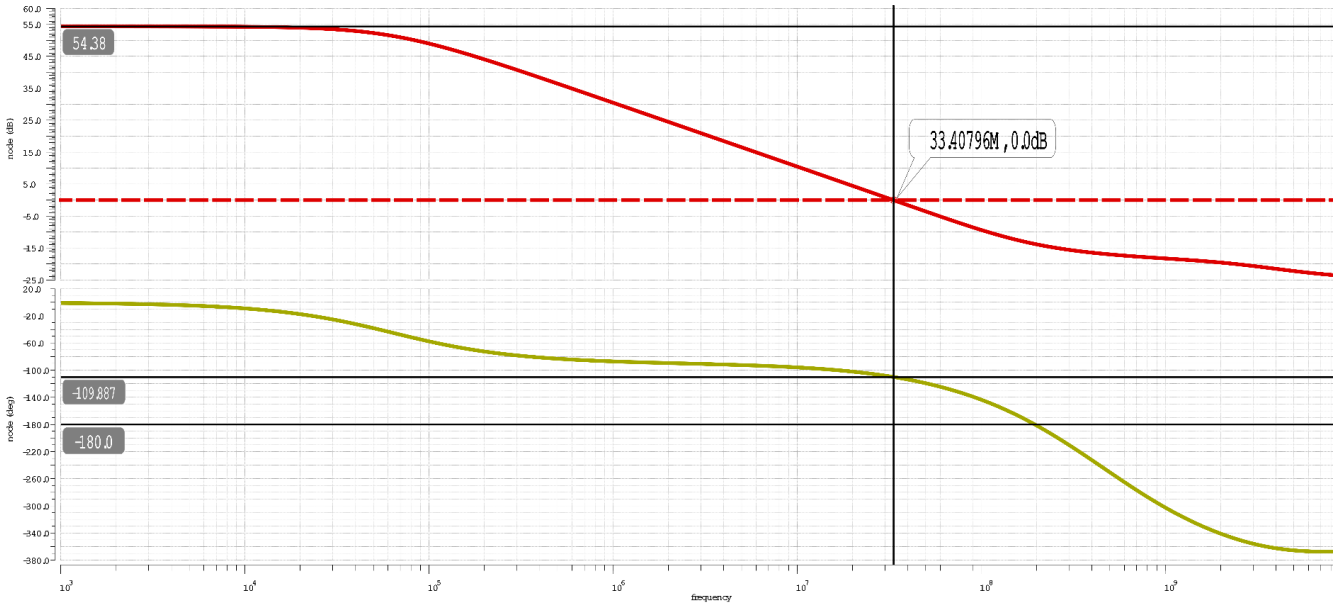
Testbench Results

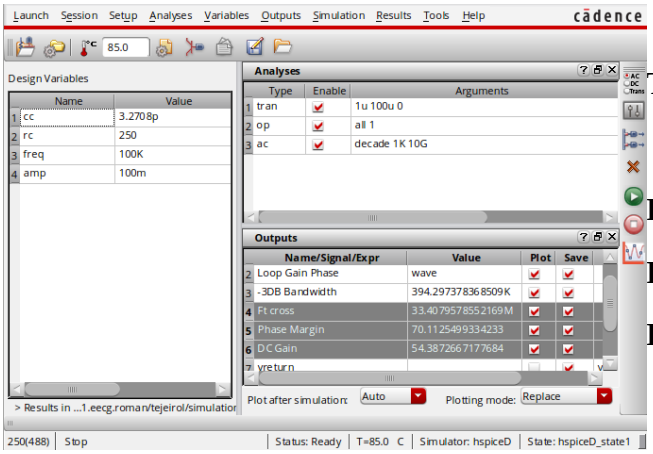
Ft = 21.039 MHz

Phase Margin = 79.081 Degrees

DC Gain = 57.525 dB

7. Fast PMOS, Slow NMOS, High Temperature, Low Voltage (FS_HT_LV) Corner





Testbench Results

Ft = 33.408MHz

Phase Margin = 70.112 Degrees

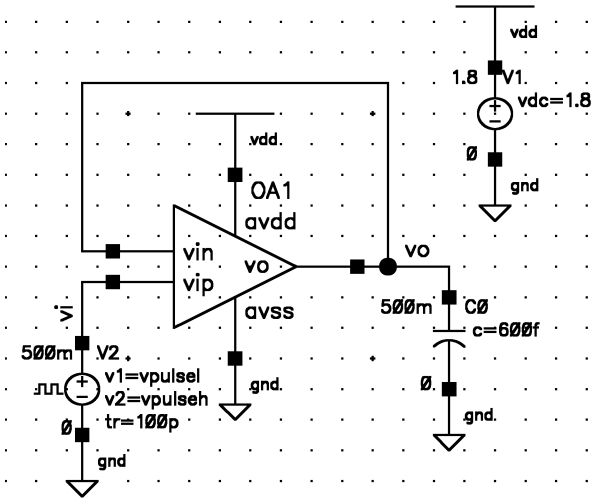
DC Gain = 54.387 dB

Summary Table

The following table summarizes our results from our corner simulation for unity gain frequency, phase margin and DC gain. (lowest and highest values for Ft, PM and DC gain are highlighted respectively)

Corner	Unity-gain Freq (MHz)	Phase Margin (Deg)	DC Gain (dB)
1. TT_TT_TV	36.350	75	55.221
2. SS_HT_LV	20.484 (lowest)	76.922	56.674
3. SS_LT_LV	28.068	77.467	55.320
4. FF_HT_HV	35.749	73.668 (lowest)	55.528
5. FF_LT_HV	43.979 (highest)	76.918	54.74
6. SF_HT_LV	21.039	79.081 (highest)	57.525 (highest)
7. FS_HT_LV	33.408	70.112	54.387 (lowest)

Finally using our **closed loop testbench**, we apply a step pulse to our input and monitor the transient response of our circuit. (See the close-loop testbench below)



Where our pulse source:

Vpulse_high = 1.1V

Vpulse_low = 500mV

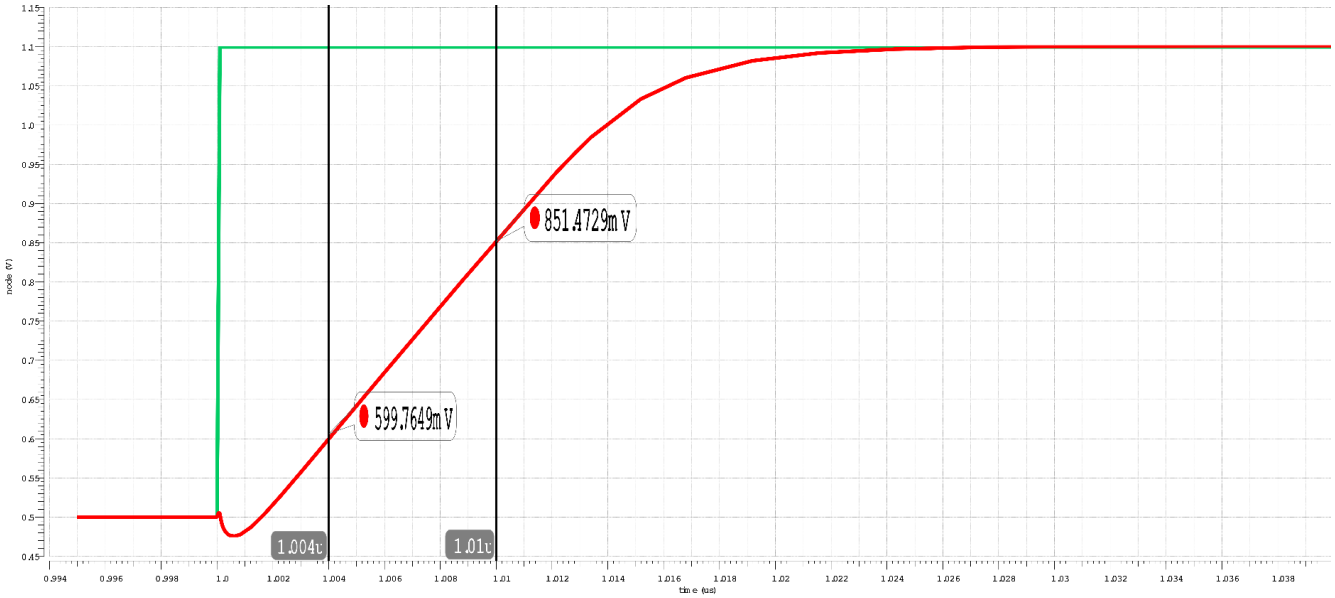
Trise = 100pS

Tfall = 100ps

Period = 1µS

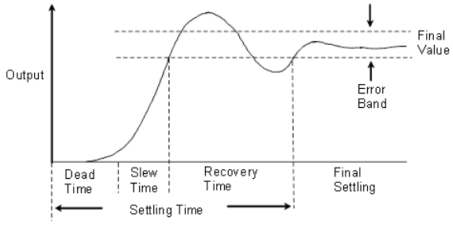
Pulse_width = 0.5µS

Then, from the transient response, as before, we need to calculate the s**lew rate (below)**, over the time window where the opamp output voltage is slewing (linear region)



$$Slew\ Rate = \frac{\Delta Vout}{\Delta time} = \frac{851.4729\,mV - 599.7649\,mV}{1.01\,\mu S - 1.004\,\mu s} = 41.952\frac{V}{\mu S} \approx 42\frac{V}{\mu S}$$

To calculate the settling time of our amplifier we recall: the settling time is the time it takes the output to respond to a step change in the input and come into, and remain within a defined error band around the final desired value. [2]



The error band is usually defined to be a percentage of the step 1%, 0.5%, 0.1%

For our amplifier transient step response we have:

For an error band of 1% of our step Vin (600mV) or 6mV error band.
$Settling\,time\,(1\%) = 1.0225661\,\mu s - 1\,\mu s = 22.566\,nS$

For an error band of 0.5% of our step Vin (600mV) or 3mV error band.
$Settling\,time\,(0.5\%) = 24.2109\,nS$

For an error band of 0.1% of our step Vin (600mV) or 600µV error band.
$Settling\,time\,(0.1\%) = 27.2448\,nS$

Because amplifier settling is not as simple as a single pole RC system, the time constant of our transient step response might not be representative for an Opamp (where many different time constants might be involved), however if a single pole approximation is assumed, we can estimate the time to reach ~63.2% of our final output value: **the approximate time constant of our circuit τ=10.6765nS.**

The amplifier power consumption is measured using our closed-loop testbench with a large sinusoidal input applied to the amplifier. Here the average current drained from the single DC power source of our system (V1) is multiplied times our supply voltage 1.8V.

Outputs

	Name/Signal/Expr	Value	Plot	Save
1	vo		☑	☑
2	vi		☑	☑
3	It		☑	☑
4	Avg Supply Current	416.106336204855u	☑	☑
5	Avg Power Consumption	748.991405168739u	☑	☑

Iavg = 416.106µA

Pavg = 748.991µW

Part 4

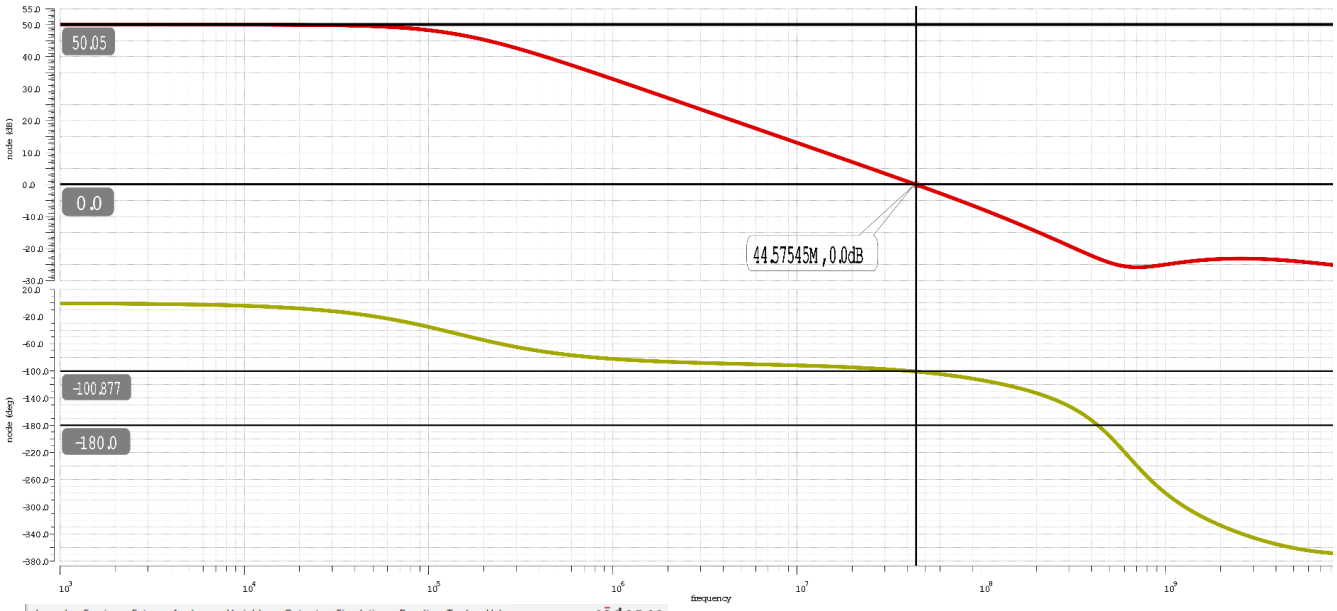
For part 4 we are asked to modify our unit transistors from part 3 such that our length is reduced to 200nm. This is is to be done while maintaining the same unity gain bandwidth and phase margin of 75 degrees.

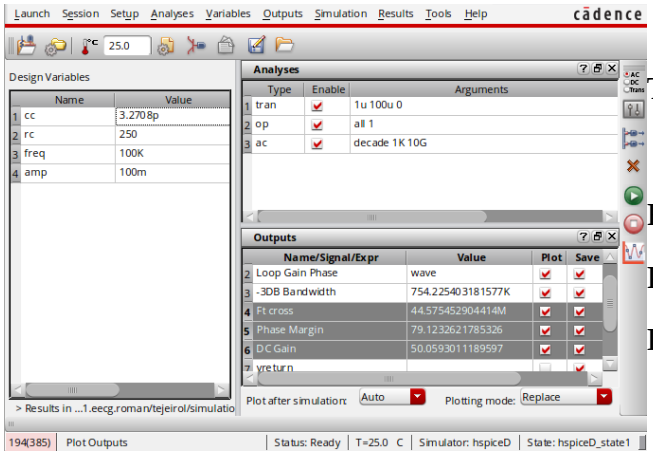
Note our equivalent W/L ratios (we are using m unit transistors in parallel) are important in setting the gm of our transistors and hence critical in setting the gain of our differential input stage and common source output stage, as well as for our mirrored bias currents and the output impedance of our active loads. To maintain a performance equivalent to our previous case (to a first order and ignoring channel length modulation effects) but now with smaller gate lengths, we should aim to maintain the W/L ratios from the original design.

Originally our unit transistor size was: W/L=2000nm/300nm=6.6667 and each of our transistors had an equivalent width equal to the number of transistors in parallel “m”. (we will leave this multiplier factor unchanged for our purposes)

Re-dimensioning our unit transistor so as to keep the W/L ratio as close to before as possible we get (using practical integer width size) $W/L = 1333\,n/200\,n \simeq 6.6650$

Upon open-loop response simulation we get Ft = 37.395MHz, PM = 76.889 degrees and A0 = 48.726dB (see bode-plot below). It’s close but not exact, because we have not accounted for second-order short-channel effects, and our W/L ratio is not exactly the same as before. (see the and initial bode-plot and results below)





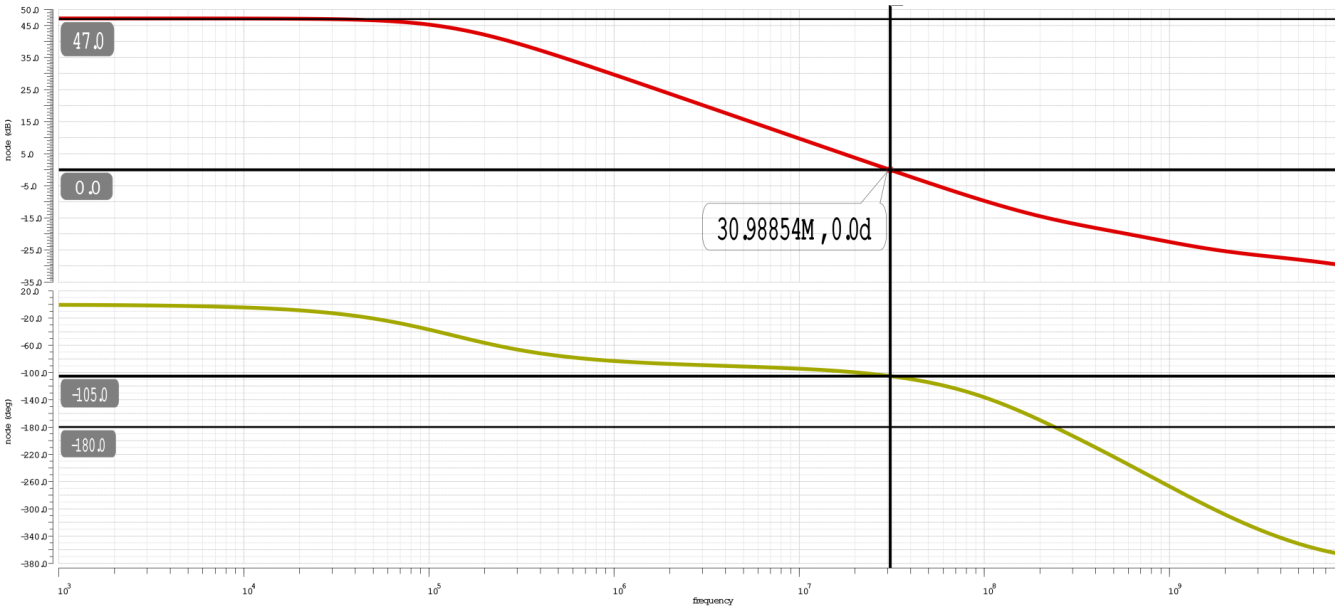
Testbench Results

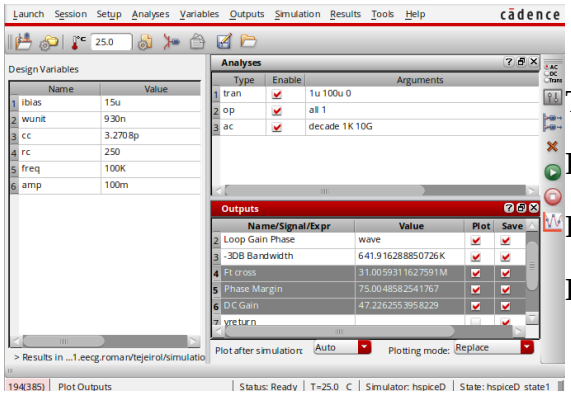
Ft = 44.575MHz

Phase Margin = 79.123 Degrees

DC Gain = 50.059 dB

To arrive at our desired phase margin of 75 degrees we need to reduce our unit width to 929.076nm which we rounded to a **practical 930nm integer size** whereby we get PM=75 degrees, Ft=31.006 MHz and A0=47.226dB: these values are very close to those measured for our Part 3 at our typical corner.





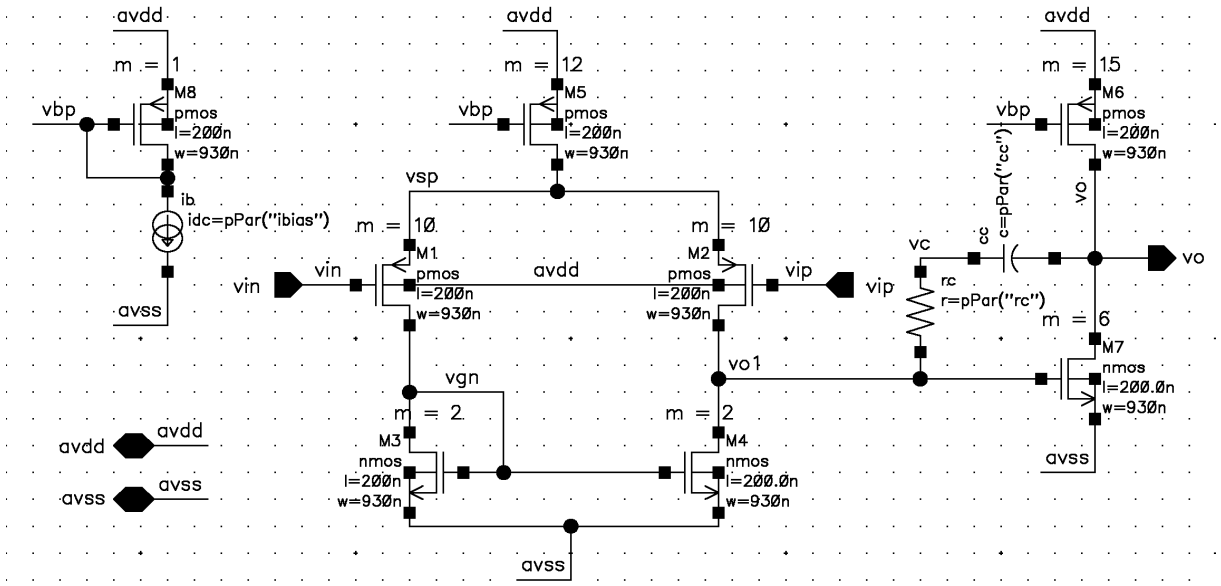
Testbench Results (more accurate)

Ft = 31.006MHz

Phase Margin = 75.005 Degrees

DC Gain = 47.226 dB (compared to 55.221dB from part 3)

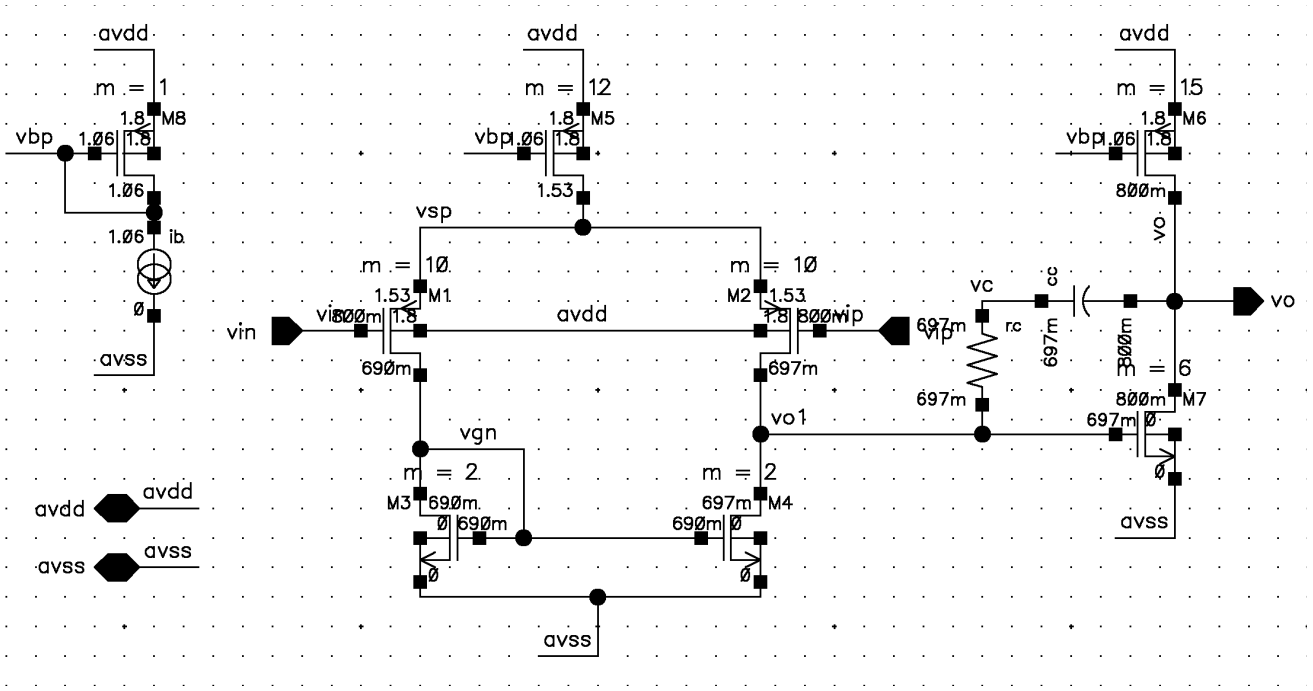
Note that interestingly we can also arrive at a 75 degrees phase margin by decreasing our DC bias current to 6.24uA while keeping our original device's unit width, however in these case our transition frequency Ft=25.389MHz which is much inferior to our required value from part 3; therefore we will be opting for the standard scaling of our unit W/L ratio found above, mainly:
W/L=930nm/200nm=4.65 The following is our schematic with all of the final device sizes annotated:



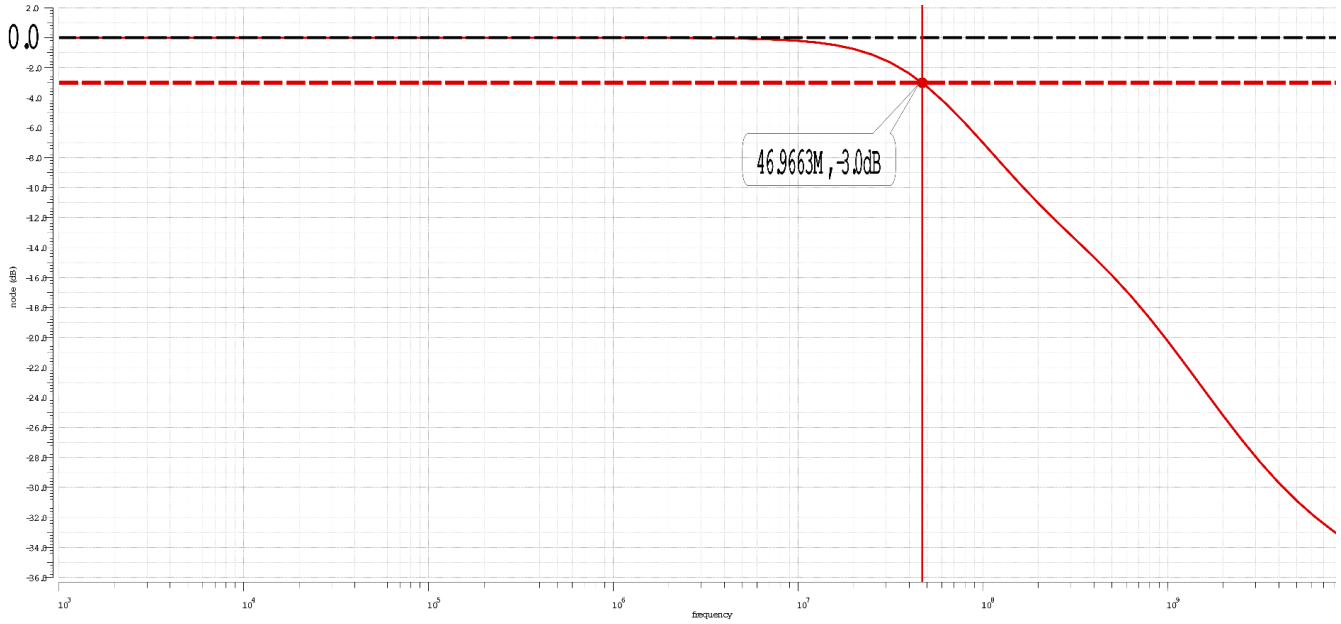
And the formatted relevant SPICE results with the DC operating point and region for all transistors. Note the underlined dc bias currents for our current-source 15µA, diff pair 149.1µA and output stage 242µA; also note the overdrive voltages "vod" underlined for all transistors.

element	1:m7	1:m4	1:m3	1:m6	1:m8	1:m5	1:m2	1:m1
model	0:nmos	0:nmos	0:nmos	0:pmos	0:pmos	0:pmos	0:pmos	0:pmos
region	**Saturati**	**Saturati**	**Saturati**	**Saturati**	**Saturati**	**Saturati**	**Saturati**	**Saturati**
id	2.422e-04	7.451e-05	7.437e-05	-2.420e-04	-1.500e-05	-1.491e-04	-7.470e-05	-7.437e-05
ibs	0.	0.	0.	0.	0.	0.	0.	0.
ibd	0.	0.	0.	0.	0.	0.	0.	0.
vgs	**6.967e-01**	**6.899e-01**	**6.899e-01**	**-7.412e-01**	**-7.412e-01**	**-7.412e-01**	**-7.292e-01**	**-7.285e-01**
vds	**8.007e-01**	**6.967e-01**	**6.899e-01**	**-9.993e-01**	**-7.412e-01**	**-2.708e-01**	**-8.324e-01**	**-8.393e-01**
vbs	0.	0.	0.	0.	0.	0.	2.708e-01	2.708e-01
vth	**4.657e-01**	**4.668e-01**	**4.668e-01**	**-4.724e-01**	**-4.737e-01**	**-4.761e-01**	**-5.539e-01**	**-5.539e-01**
vdsat	**1.691e-01**	**1.648e-01**	**1.647e-01**	**-2.221e-01**	**-2.212e-01**	**-2.195e-01**	**-1.630e-01**	**-1.625e-01**
vod	**2.311e-01**	**2.231e-01**	**2.230e-01**	**-2.688e-01**	**-2.675e-01**	**-2.651e-01**	**-1.753e-01**	**-1.746e-01**
beta	1.095e-02	3.649e-03	3.649e-03	6.380e-03	4.252e-04	5.099e-03	4.147e-03	4.147e-03
gam eff	5.686e-01	5.686e-01	5.686e-01	4.350e-01	4.350e-01	4.350e-01	4.187e-01	4.187e-01
gm	**1.842e-03**	**5.933e-04**	**5.927e-04**	**1.552e-03**	**9.812e-05**	**9.764e-04**	**7.232e-04**	**7.218e-04**
gds	6.041e-05	1.989e-05	1.992e-05	6.450e-05	4.501e-06	1.111e-04	2.560e-05	2.544e-05
gmb	4.333e-03	1.231e-03	1.219e-03	4.752e-04	3.002e-05	2.991e-04	2.028e-04	2.024e-04
cdtot	3.769e-15	1.257e-15	1.257e-15	9.469e-15	6.314e-16	7.680e-15	6.311e-15	6.311e-15
cgtot	1.380e-14	4.601e-15	4.601e-15	3.303e-14	2.202e-15	2.649e-14	2.190e-14	2.190e-14
cstot	1.207e-14	3.797e-15	3.782e-15	1.660e-14	1.107e-15	1.329e-14	1.093e-14	1.092e-14
cbtot	-9.665e-16	-1.969e-16	-1.886e-16	3.723e-15	2.482e-16	3.006e-15	2.197e-15	2.197e-15
cgs	2.268e-14	6.984e-15	6.946e-15	2.329e-14	1.553e-15	1.864e-14	1.545e-14	1.545e-14
cgd	3.731e-15	1.244e-15	1.244e-15	9.426e-15	6.285e-16	7.628e-15	6.281e-15	6.281e-15

Additionally, see the **annotated schematic with DC node voltages** (also available from results above)



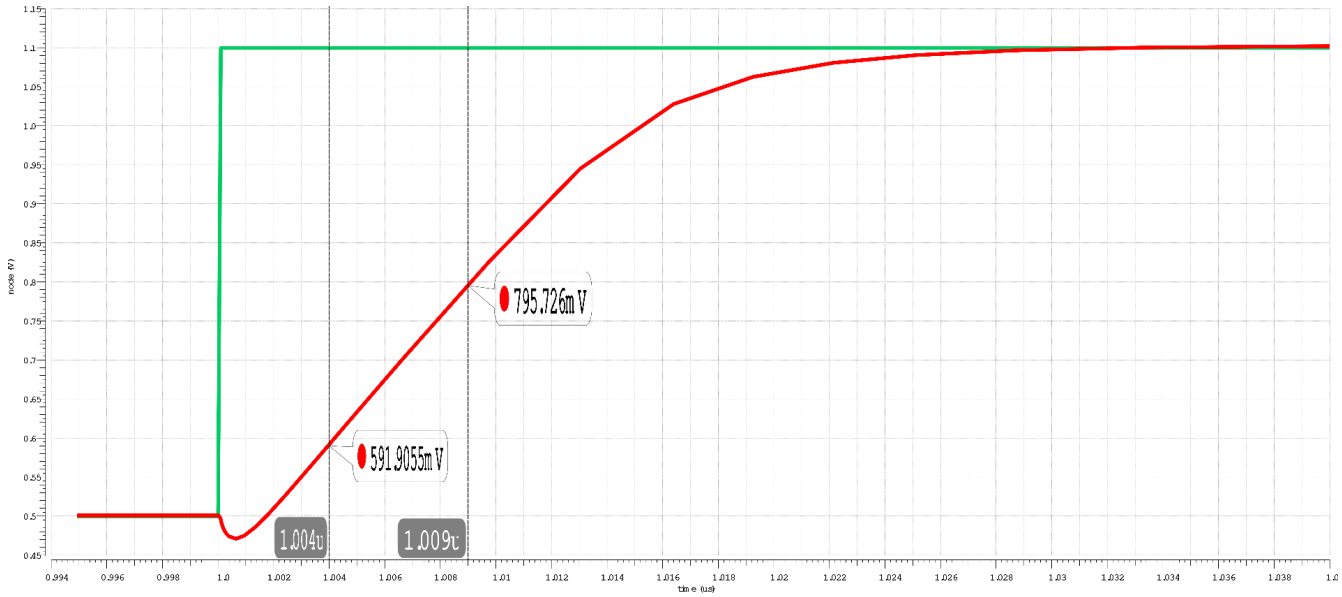
The **bode-plot for the closed-loop testbench** can be found below.



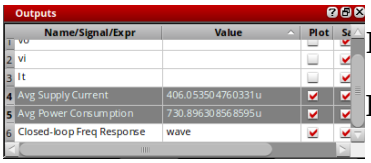
Note that our **closed-loop DC gain A0=0dB** (as we should expect given a unity gain configuration), and our **3db bandwidth F3db=46.966MHz.**

Subsequently the **slew rate for our unity-gain closed-loop amplifier** (from our step response transient simulation, see plot below) (**same testbench as that used for part 3**)

$$Slew\ Rate = \frac{\Delta Vout}{\Delta time} = \frac{795.726\,mV - 591.9055\,mV}{1.004\,\mu S - 1.009\,\mu s} = 40.764\,\frac{V}{\mu S}$$



And our **supply current and power consumption** (same measurement testbench as before):



Iavg = 406.053µA

Pavg = 730.896µW

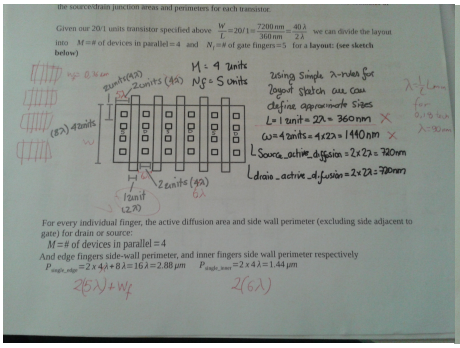
It is worth nothing that even though we are employing roughly the same average power, in our case the reduction in gate length and our subsequent re-sizing of our unit devices to maintain the same phase margin of 75 degrees, has resulted in a degradation of our open-loop DC gain of approximately 8dB with a slight decrease in our unity gain frequency. Additionally, in our transient step response in closed-loop configuration, we also see a small decrease in the slew rate.

References

[1] Analog Artist with HSPICE: https://www.eda.ncsu.edu/wiki/Tutorial:Analog_Artist_with_HSPICE

[2] Opamp Settling Time: https://wiki.analog.com/university/courses/electronics/electronics-lab-1st

ERRATA



the source/drain junction areas and perimeters for each transistor.

Given our 20/1 units transistor specified above $\frac{W}{L}=20/1=\frac{7200\,nm}{360\,nm}=\frac{40\lambda}{2\lambda}$ we can divide the layout into $M=\#$ of devices in parallel = 4 and $N_f=\#$ of gate fingers = 5 for a **layout: (see sketch below)**

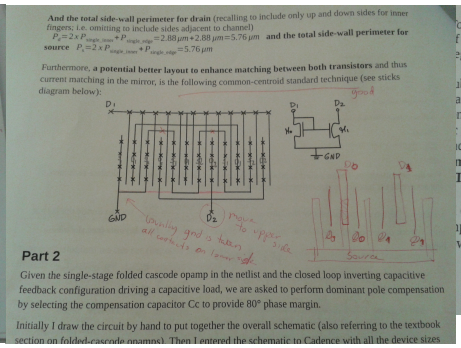
M = 4 units
N_f = 5 units
using Simple λ-rules for layout sketch our can define approximate sizes
L = 1 unit = 2λ = 360nm
W = 4 units = 4x2λ = 1440nm
$L_{source\_active\_diffusion}$ = 2x2λ = 720nm
$L_{drain\_active\_diffusion}$ = 2x2λ = 720nm

For every individual finger, the active diffusion area and side wall perimeter (excluding side adjacent to gate) for drain or source:

$M=\#$ of devices in parallel = 4

And edge fingers side-wall perimeter, and inner fingers side wall perimeter respectively

$P_{single\_edge}=2\times4\lambda+8\lambda=16\lambda=2.88\,\mu m$ $P_{single\_inner}=2\times4\lambda=1.44\,\mu m$



And the total side-wall perimeter for drain (recalling to include only up and down sides for inner fingers; i.e. omitting to include sides adjacent to channel)

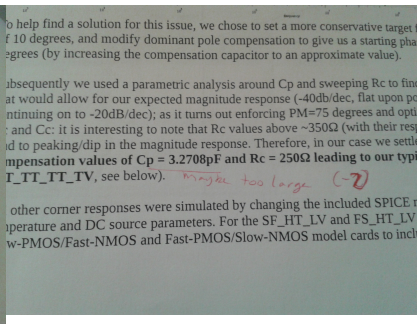
$P_D=2\times P_{single\_inner}+P_{single\_edge}=2.88\,\mu m+2.88\,\mu m=5.76\,\mu m$ **and the total side-wall perimeter for source** $P_S=2\times P_{single\_inner}+P_{single\_edge}=5.76\,\mu m$

Furthermore, **a potential better layout to enhance matching between both transistors** and thus current matching in the mirror, is the following common-centroid standard technique (see sticks diagram below):

Part 2

Given the single-stage folded cascode opamp in the netlist and the closed loop inverting capacitive feedback configuration driving a capacitive load, we are asked to perform dominant pole compensation by selecting the compensation capacitor Cc to provide 80° phase margin.

Initially I draw the circuit by hand to put together the overall schematic (also referring to the textbook section on folded-cascode opamps). Then I entered the schematic to Cadence with all the device sizes



o help find a solution for this issue, we chose to set a more conservative target
f 10 degrees, and modify dominant pole compensation to give us a starting pha
egrees (by increasing the compensation capacitor to an approximate value).

bsequently we used a parametric analysis around Cp and sweeping Rc to fin
at would allow for our expected magnitude response (-40db/dec, flat upon po
ntinuing on to -20dB/dec); as it turns out enforcing PM=75 degrees and opti
and Cc: it is interesting to note that Rc values above ~350Ω (with their resu
d to peaking/dip in the magnitude response. Therefore, in our case we settl
mpensation values of Cp = 3.2708pF and Rc = 250Ω leading to our typi
T_TT_TT_TV, see below).

other corner responses were simulated by changing the included SPICE
perature and DC source parameters. For the SF_HT_LV and FS_HT_LV
w-PMOS/Fast-NMOS and Fast-PMOS/Slow-NMOS model cards to incl