8-bit Time-Interleaved ADC Simulation and Characterization

1. Preparation: As required the chapter 17 of the textbook and the course slides were reviewed for this assignment. *Note there was an error in the INL formula described for the previous assignment corrected here.*

2. 8-bit ADC Simulation and Characterization:

First, the 8-bit ADC test-bench was put together as required in the assignment write-up, with a 1.1V reference and clock signal at Fs=8GHz (in my case) with 5pS rise and fall times. Subsequently an ideal 8-bit DAC was used to convert the binary code generated by the ADC back to the analog domain for taking measurements. (see figure 2 for ADC test-bench)

2a. INL and DNL measurements (0% mismatch factor)

Initially a modified version of the adc_inl and adc_dnl measurement blocks from the ahdl library were used, however the measured ideal ADC INL and DNL results were incorrect (when compared to both by-hand post-processing and expectations from the reference textbook and on-line sources). Hence, we opted for manual post-processing of the DAC analog output data using spreadsheet software (LibreOffice Calc) to compute the INL and DNL measurements for our ADC.

The normal set-up to measure INL and DNL is to provide a ramp input to the ADC under test, here with a clock of 8GHz (or 1 sample converted every 125pS) and given 8 bits of resolution, we have to cover 2^N or 256 samples. Therefore, the rise time for our input waveform $t_{rise} \geq 125\,pS\,x\,256 = 32\,nS$ to cover every digital code or conversion step. (See figure 2a1 for the input ramp and DAC output steps waveform)

We then exported the raw DAC output data to a CSV file through the results explorer and post-processed the data with spreadsheet software , basically: (1) Flag and copy only a single sample from each DAC output step and (2) enumerate the copied samples with appropriate digital codes from 0 to 255. (this manual cleanup process was made simple by appropriately choosing the ramp properties above)

Calculating INL and DNL (based on book definition)

(INL definition from previous assignment corrected here)

The Integral Non-linearity (INL) is the output response deviation from a straight line (after both offset and gain errors have been removed). Here the difference between the straight line and the DAC output voltage at every digital code (in LSBs) is the INL. Hence for our data, to be able to compute the INL, we have to remove gain and offset errors, then we would be able to compare with the ideal (straight line) response. Thus removing gain and offset errors for each sample (Here V_{LSB} is the ideal value):

$$V[\text{current\_code}]_{LSB} = \frac{V[\text{current\_code}]}{V_{LSB}} - E_{offset} - \left(\frac{\text{current\_code}}{2^N - 1}\right) x\, E_{gain}$$

where in our case (ideal ADC with no mismatch):

$$E_{offset} = V[0]/V_{LSB} = 0\,LSB$$

$$E_{gain} = \frac{V[\text{last\_code}] - V[0]}{V_{LSB}} - \text{last\_code} = 0\,LSB$$

Hence, for our ideal ADC case our offset-free gain-free values are the same as our measured values. Therefore we can calculate our INL (all done in LSB units) as the difference between each measured current code and the ideal code (for every step):

$$INL = \frac{V'[\text{current\_code}]}{V_{LSB}} - \text{ideal\_code} = V'[\text{current\_code}]_{LSB} - \text{ideal\_code}$$

Now the definition of the cadence INL measurement block from our previous assignment is precisely equivalent but here the LSB voltage is the "measured" LSB voltage (INL Cadence measurement block definition):

$$INL = \frac{V[\text{current\_code}]}{V'_{LSB}} - \text{ideal\_code} = V'[\text{current\_code}]_{LSB} - \text{ideal\_code}$$

Having the INL measurement, calculating the DNL equates to just taking the difference from adjacent INL measurements. Alternatively one can compute the DNL – as the difference in the step size from the ideal step size – directly from the offset-free gain-free values as follows (equivalent book definition and Cadence DNL measurement block definition respectively):

$$DNL = \frac{(V'[\text{next\_code}] - V'[\text{current\_code}]) - V_{LSB}}{V_{LSB}} = Vstep_{LSB} - 1\,LSB$$

$$DNL = \frac{(V[\text{next\_code}] - V[\text{current\_code}]) - V'_{LSB}}{V'_{LSB}} = Vstep_{LSB} - 1\,LSB$$

(It was this DNL formula that was mislabeled as INL in assignment 5)

For our ideal ADC with 0 mismatch, we can see our INL is below +/- 0.5 LSB and the DNL is below 1 LSB indicating ideal performance. (see figures 2a2 and 2a3 for the measured INL and DNL respectively).

2b. INL and DNL Measurements (1% mismatch factor)

In this next question we are asked to provide a 1% mismatch factor to the ADC block. Inspecting the source for the cell we can see first that the implementation of the ADC block is of an algorithmic type:

- If Vin is greater than half Vref: the bit is set to 1 and half Vref is subtracted from the input then doubled, the result is then re-applied to the input.
- If Vin is lower than half Vref: the bit is unset to 0 and the input voltage is doubled, the result then is re-applied to the input.

We can also see that the mismatch factor represents a small random error in the comparator reference voltage proportional to the percent of mismatch provided as a parameter to the block. This effect is analogous to random offset present in a comparator, which if significant enough can lead to the comparator outputting a 0 when it should have been a 1 for the LSBs (the smallest input amplitudes), giving rise to missing codes for the ADC.

Subsequently we plotted the response of the non-ideal ADC to the same input ramp as before (see figure 2b1 for the input ramp and DAC output steps waveform and figures 2b2 and 2b3 for the measured INL and DNL respectively), from our transient response we can see there are some missing steps or missing codes due to the 1% mismatch factor, equivalently we can see the INL and DNL measurements are lower than -0.5 LSB and equal to -1 LSB respectively at 3 digital codes: 3, 104 and 205.

2c. SNDR and ENOB vs. Input Amplitude

For this section we vary the input signal amplitude from 2.5 mV to 550mV (steps chosen: 2.5mV, 25mV, 250mV and 550mV) keeping the input frequency at 100MHz. Then we compute the SNDR as

for previous assignments (fundamental minus largest harmonic in dB) and the ENOB as: $ENOB = (SNDR - 1.76\,dB)/6.02$ (see figure 2c1 for the transient response and DFT at the output at a 550mV input amplitude, see figures 2c2 and 2c3 for the SNDR and ENOB vs. input amplitude). The ENOB at full scale for our ADC with the 1% mismatch factor is 5.829 bits.

2d. SNDR and ENOB vs. Input Frequency

Next, we vary the input frequency from 100MHz to 6.1GHz keeping the input amplitude at full scale 550mV, then we compute the SNDR and ENOB as before (See figures 2d1 and 2d2 for the SNDR and ENOB vs. input frequency). Lastly we compute the effective resolution bandwidth: frequency over which a converter's peak SNDR is within 3db (or ENOB within 0.5 bits) of it's peak value. From the slope of the first two frequency points taken, the point at which the ENOB is 0.5 bits less than that the peak is: $BW_{eff} = 244.134\,MHz$

3. 2x Time-int. 8bit ADC Simulation and Characterization

For this section the setup was exactly as before with a couple of added components: an additional ADC channel (and test DAC), non-overlapping clock signals – 5pS rise and fall times, 25% duty cycles (31.25pS) and a delay of half a period (62.5pS) for the second interleaved channel – and finally an ideal analog multiplexer (analog_mux from ahdlLib) was used to combine both DAC analog outputs. (See figure 3 for the ADC testbench)

3a. INL and DNL measurements (1% mismatch factor)

Here to provide a ramp input to the ADC under test, we have to remember that a 2x interleaved ADC can convert two samples every Fs = 8GHz clock cycle (i.e. 2 samples for every 125pS), this is equivalent to a single ADC with Fs = 16GHz (or 1 sample every 62.5pS). Now given 8 bits of resolution, we have to cover 2^N or 256 samples. Therefore, the rise time for our input waveform $t_{rise} \geq 62.5\,pS\,x\,256 = 16\,nS$ to cover every digital code or conversion step. (See figure 3a1 for the input ramp and DAC output steps waveform)

Then, we exported the raw DAC output data to a CSV file and post-processed the data with spreadsheet software to calculate the INL and DNL error measurements (same procedure as section 2a) for our time-interleaved ADC (See figures 3a2 and 3a3 for the measured INL and DNL respectively). Here as before, we can see there are some missing steps or missing codes due to the 1% mismatch factor, or equivalently we can see the INL and DNL measurements lower than -0.5 LSB and equal to -1 LSB respectively at 3 digital codes. It is worth nothing however that while we have some missing codes as before, we are operating at effectively twice the input frequency for our ramp.

3b. SNDR and ENOB vs. Input Frequency

Next we are asked to calculate the SNDR and ENOB vs frequency from 100MHz to 6.1GHz keeping the input amplitude at full scale 550mV (See figure 3b1 for the transient response and DFT of the output at a 550mV input amplitude, see figures 3b2 and 3b3 for the SNDR and ENOB vs. input frequency). Then, from the slope of the first two frequency points, the point at which the ENOB is 0.5 bits less than that the peak is: $BW_{eff} = 231.856\,MHz$. This result can be misleading however, for instance it does not take into account that the starting ENOB (or equivalently SNDR) at 100MHz for the time-interleaved ADC is 7.477 bits as compared to 5.829 bits for the single ADC. A better measure to assess the performance comparison of both ADCs is to compare the SNDR and ENOB figures of merit at each test frequency.

In the case of the single ADC for example the SNDR drops below 0dB at 4.1GHz (which means the input signal can not be recovered and it is indistinguishable from the distortion harmonics) as expected given Fs/2 is 4GHz, and even looking at 1.1GHz we can start to see some aliasing in the transient response with the ENOB figure dropping below 2.5 bits; at the greater frequencies of 2.1 and 3.1GHz aliasing becomes very prominent with the ENOB figure nearing 1.5 bits.

For the 2x time-interleaved ADC on the other hand the SNDR remains positive (11.787dB) all the way up to 6.1GHz as expected given that our effective Nyquist frequency is now 8GHz, our ENOB figure drops below 2.5 bits only after 3.1GHz where we start to see some aliasing in the transient response and aliasing becomes more prominent only after 4.1GHz.

Compared to the output of a single DAC, the combined output of the two DACs (the time-interleaved ADC) is effectively as if we had a single ADC clocked at twice the actual sampling frequency or Fs = 2Fs = 16GHz, this is because each interleaved ADC samples the input signal half a period after the other ADC, together taking two samples per sampling period: effectively doubling the sampling clock or equivalently the bandwidth of analog input signals that can be converted to a digital representation.

Hence to conclude, with our 2x time interleaved ADC, we have effectively doubled sampling rate – the bandwidth of input frequencies our ADC can process – the ENOB at full-scale and low frequencies (100MHz) is only 0.5 bits below the 8bits on-paper-spec, and the SNDR and ENOB FoMs are much superior at every test frequency than those measured from our single ADC; here our results match our expectation for a 2x time-interleaved converter.

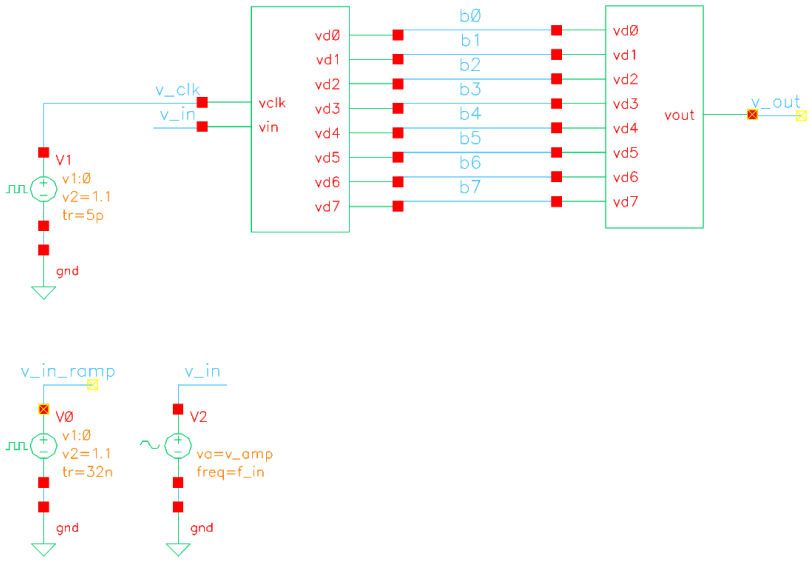

Figure 2: Single ADC simple test-bench

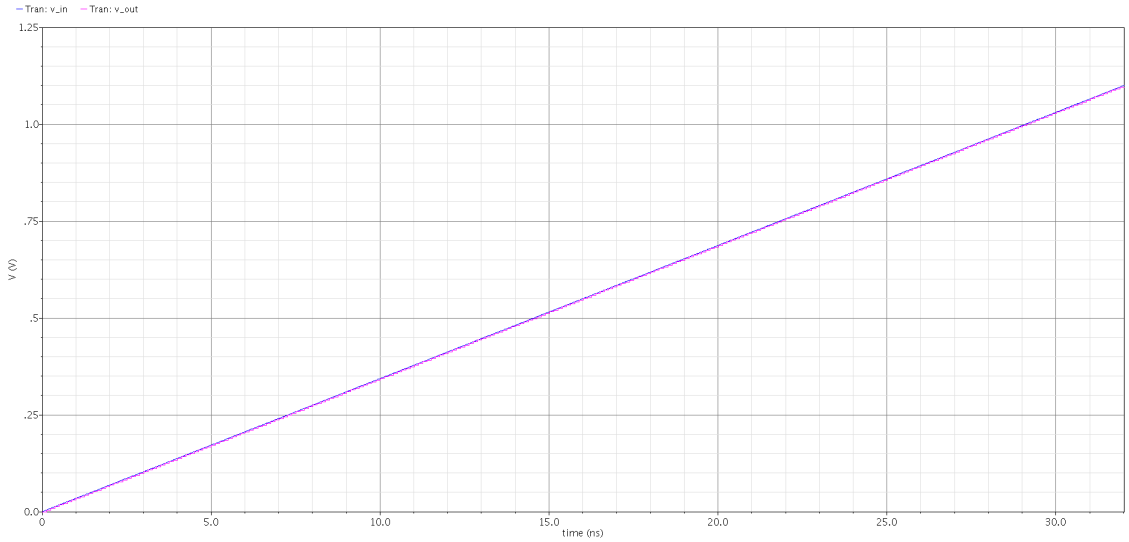

Figure 2a1: Input ramp and DAC output steps waveform (no mismatch)

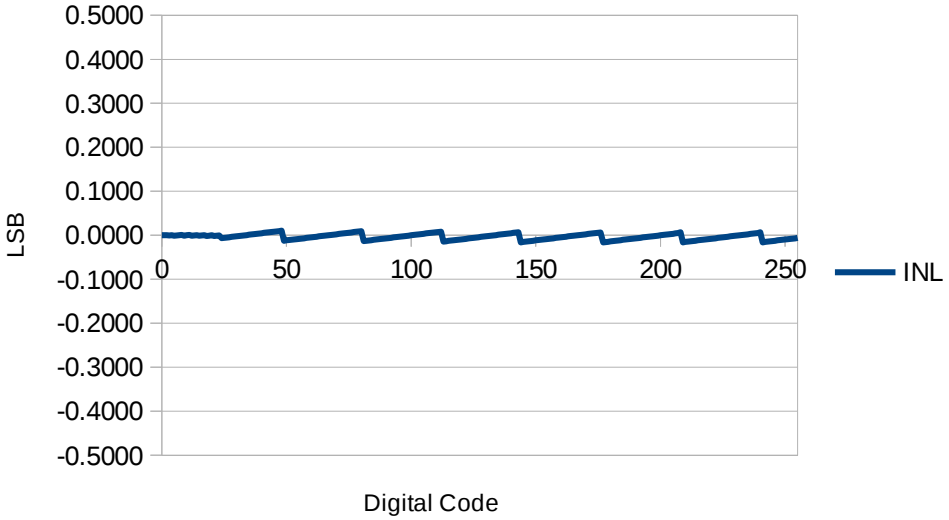

Figure 2a2: Measured INL for single ADC (no mismatch)

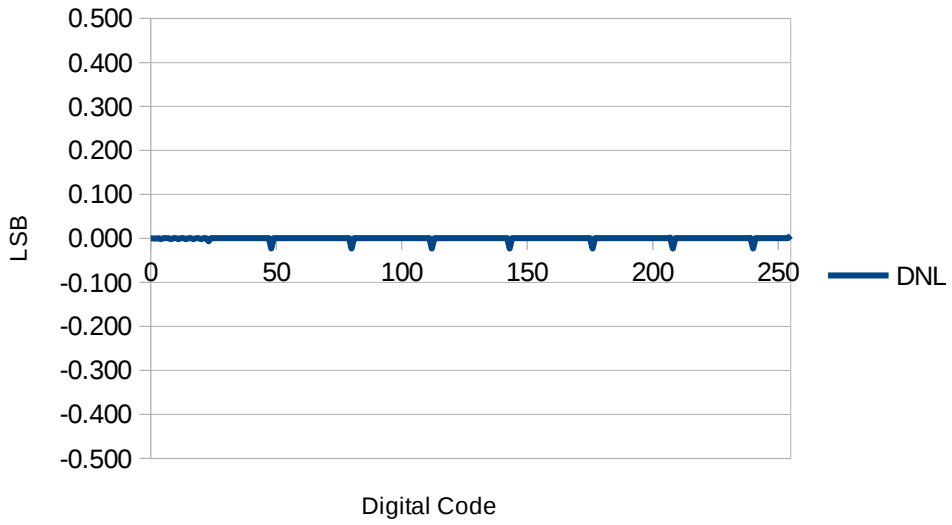

Figure 2a3: Measured DNL for single ADC (no mismatch)

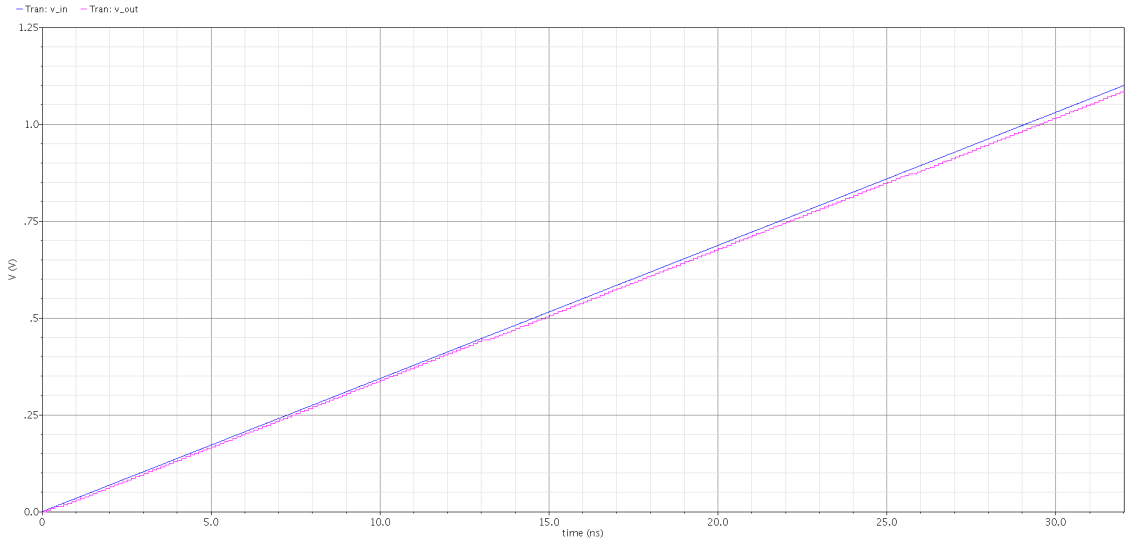

Figure 2b1: Input ramp and DAC output steps waveform (1% mismatch)

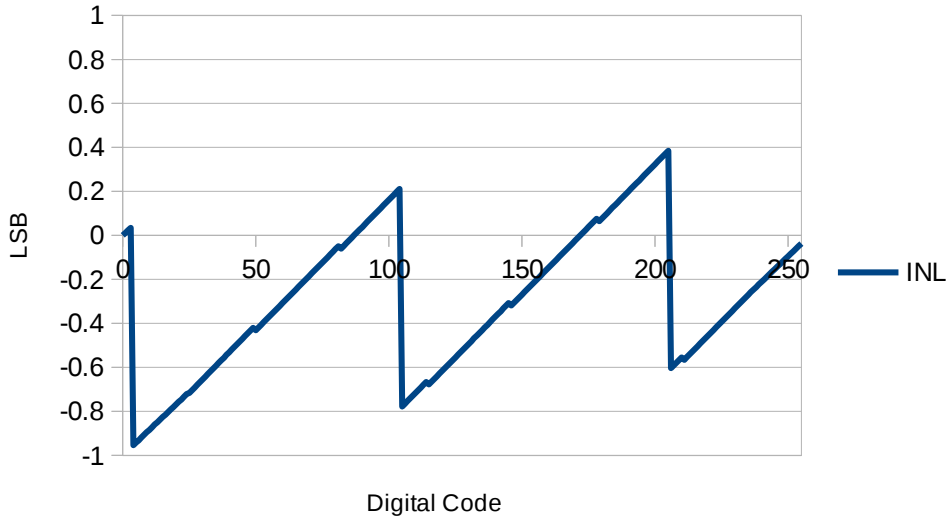

Figure 2b2: Measured INL for single ADC (1% mismatch)

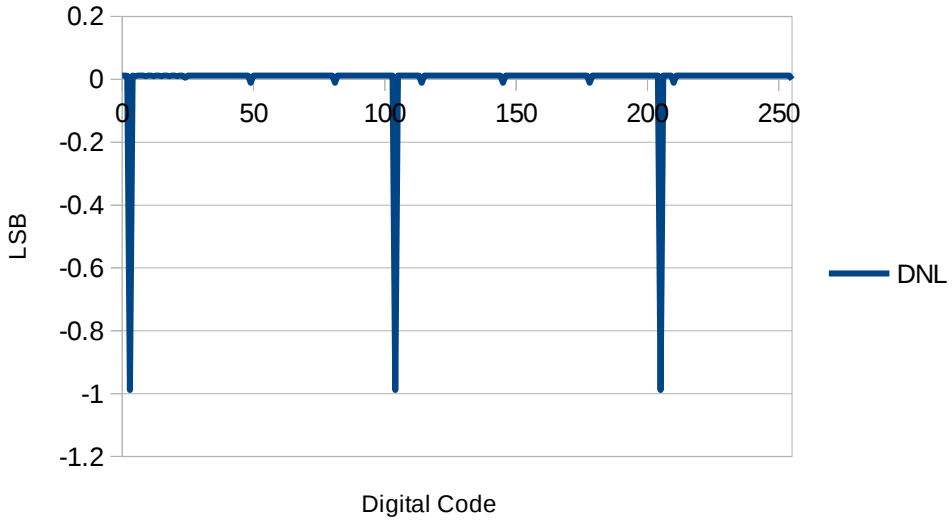

Figure 2b3: Measured DNL for single ADC (1% Mismatch)

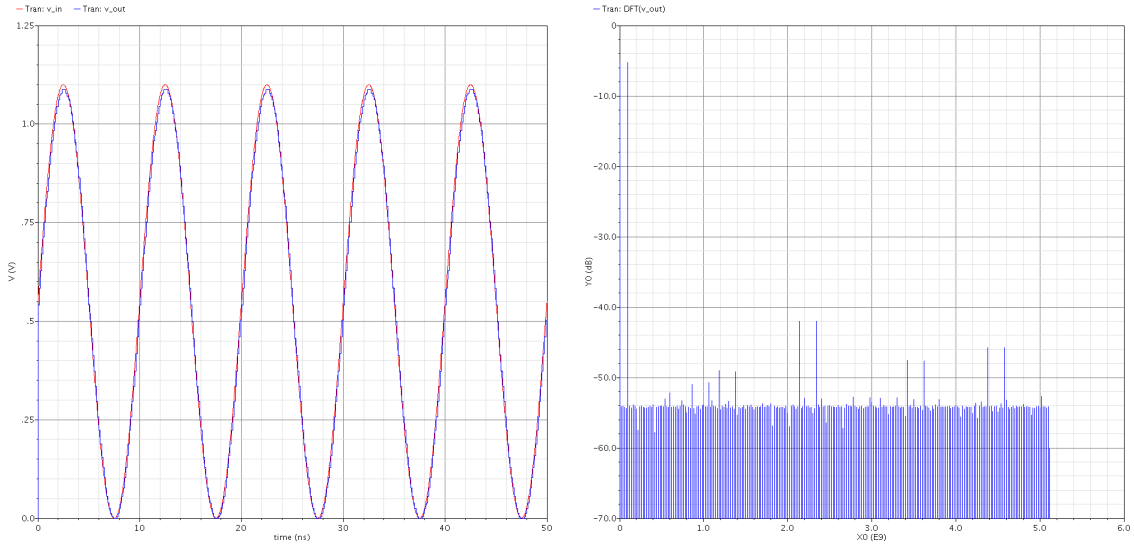

Figure 2c1: Transient response and DFT at the output at 100MHz and a 550mV input amplitude (for reference)

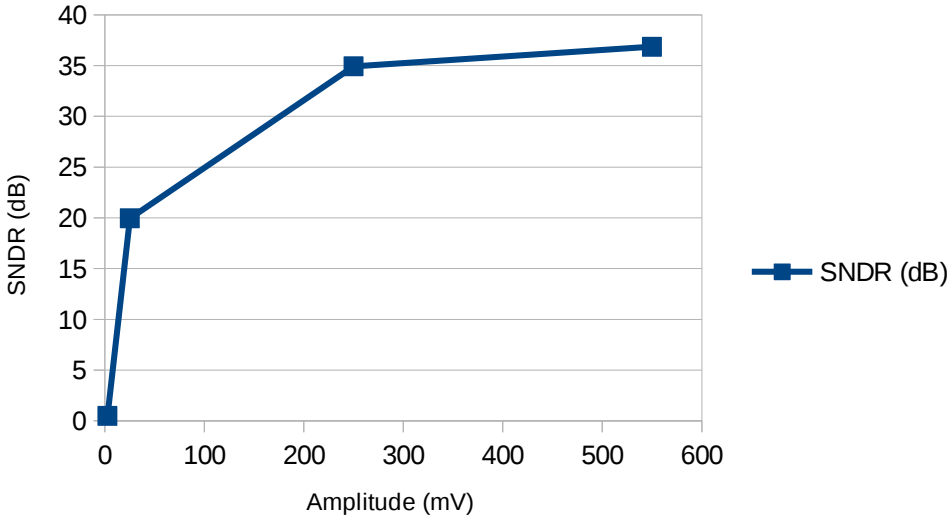

Figure 2c2: SNDR vs. input amplitude

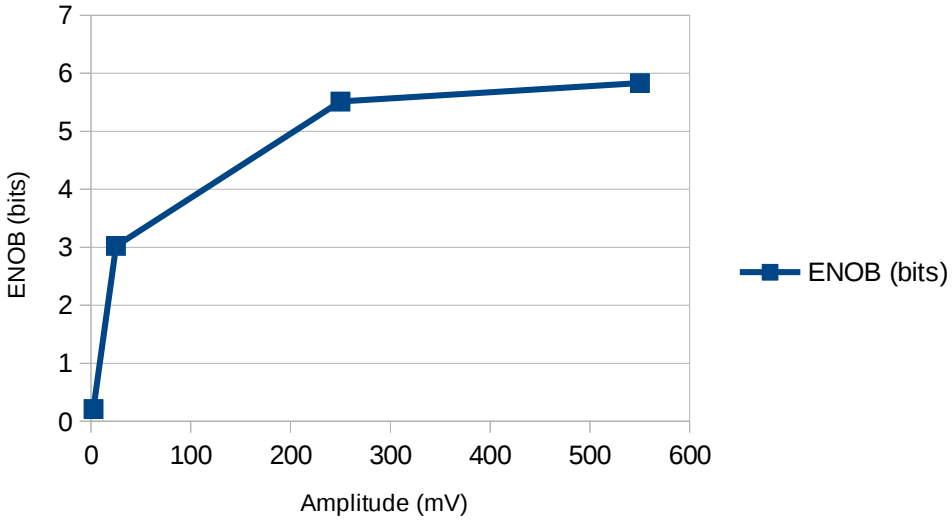

Figure 2c3: ENOB vs. input amplitude

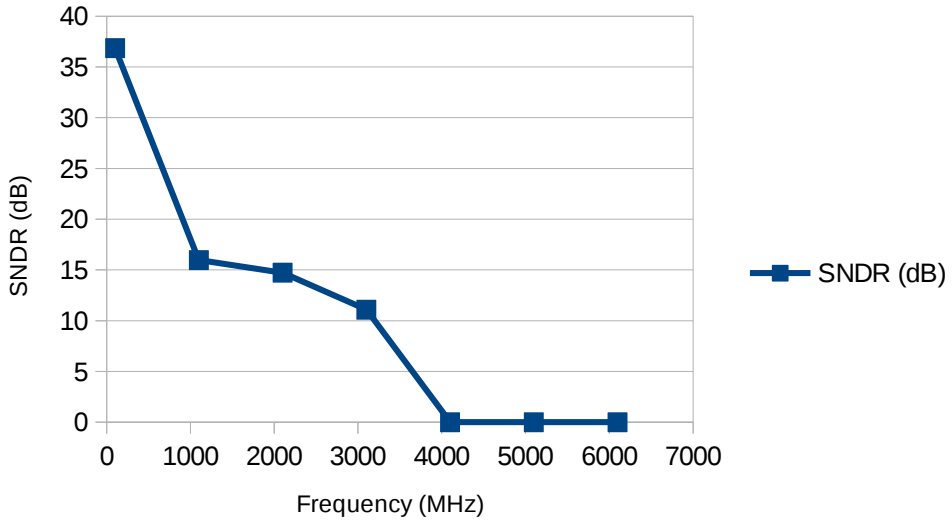

Figure 2d1: SNDR vs. input frequency

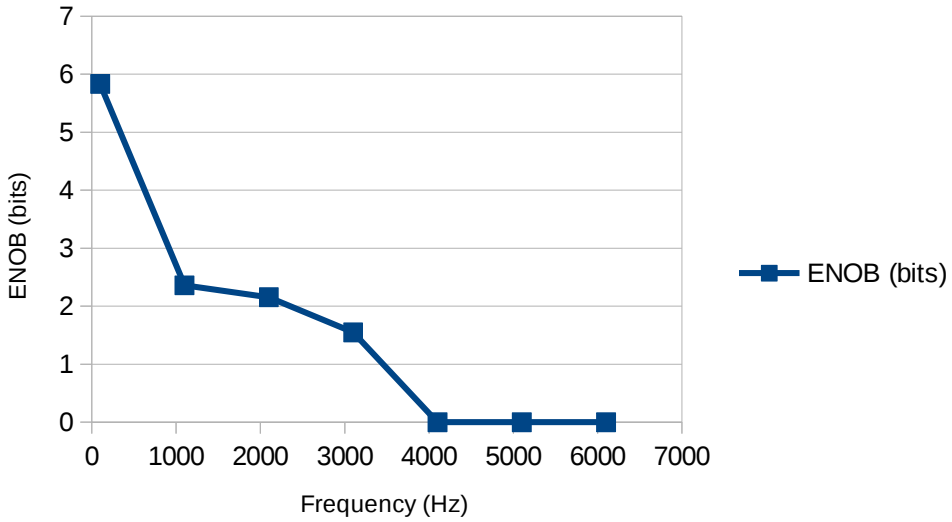

Figure 2d2: ENOB vs. input frequency

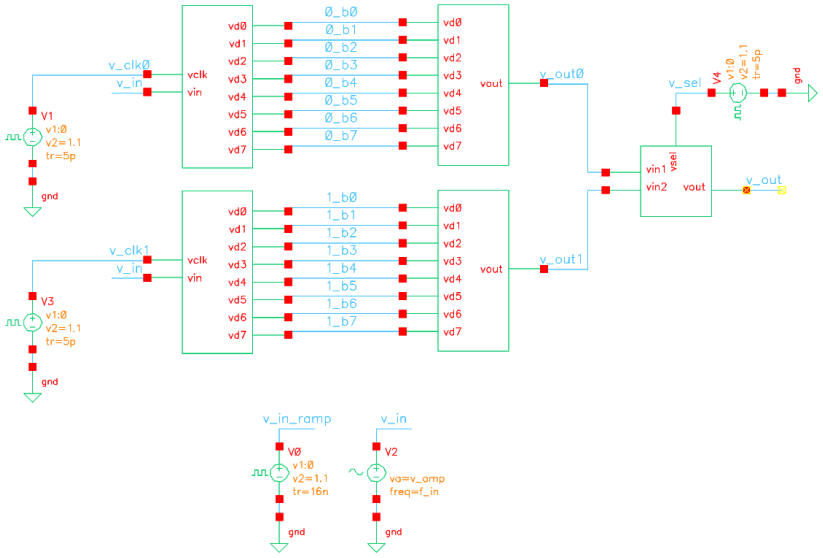

Figure 3: 2x time-interleaved ADC test-bench

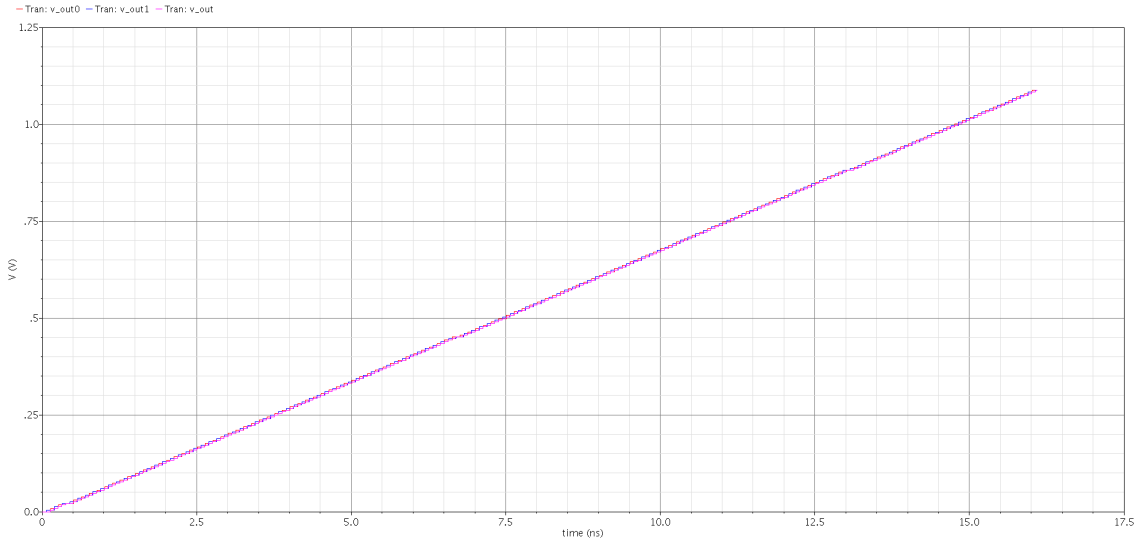

Figure 3a1: DAC output steps waveform (note the time-scale is half as compared to before, mismatch 1%)

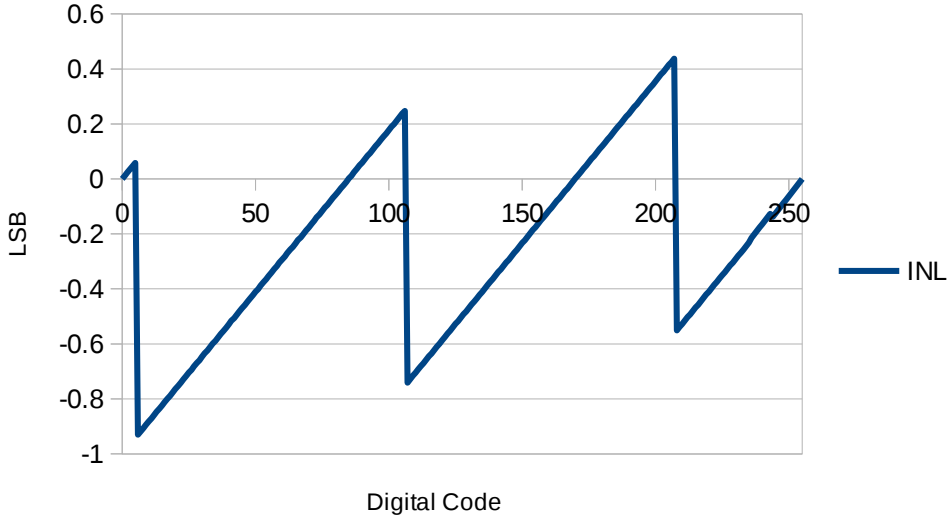

Figure 3a2: Measured INL for time-interleaved ADC (1% mismatch)

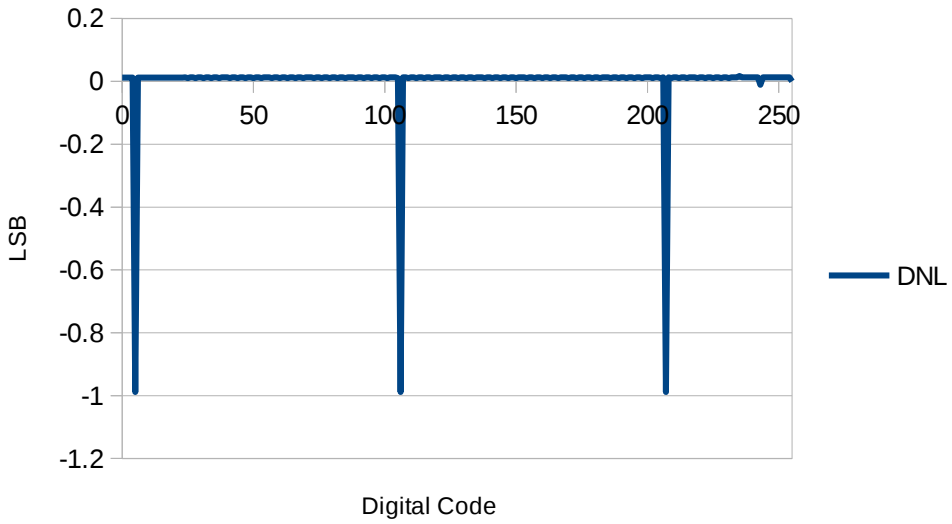

Figure 3a3: Measured DNL for time-interleaved ADC (1% mismatch)

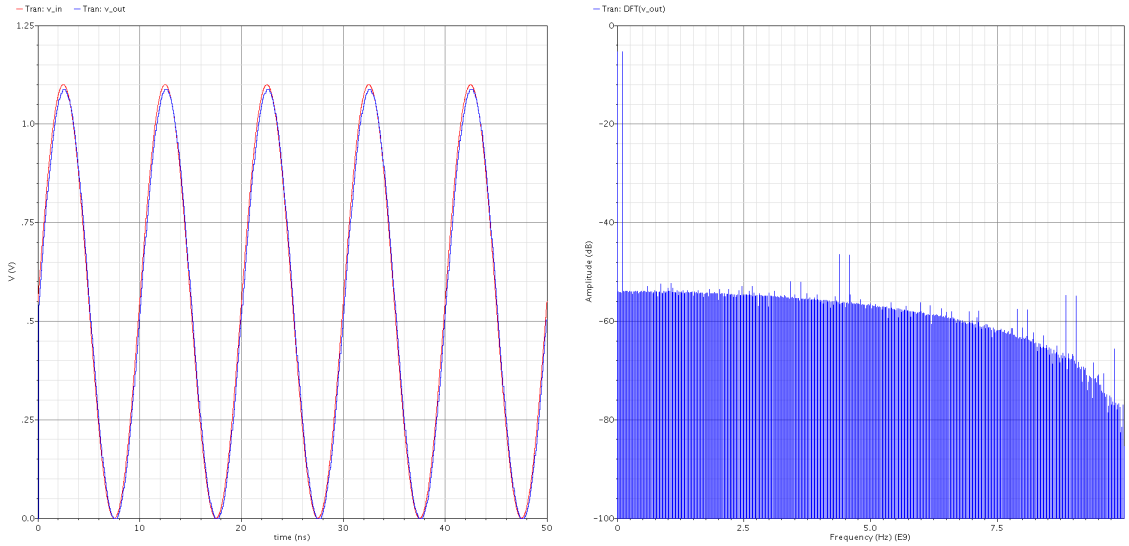

Figure 3b1: Transient response and DFT at the output at 100MHz and a 550mV input amplitude (for reference)

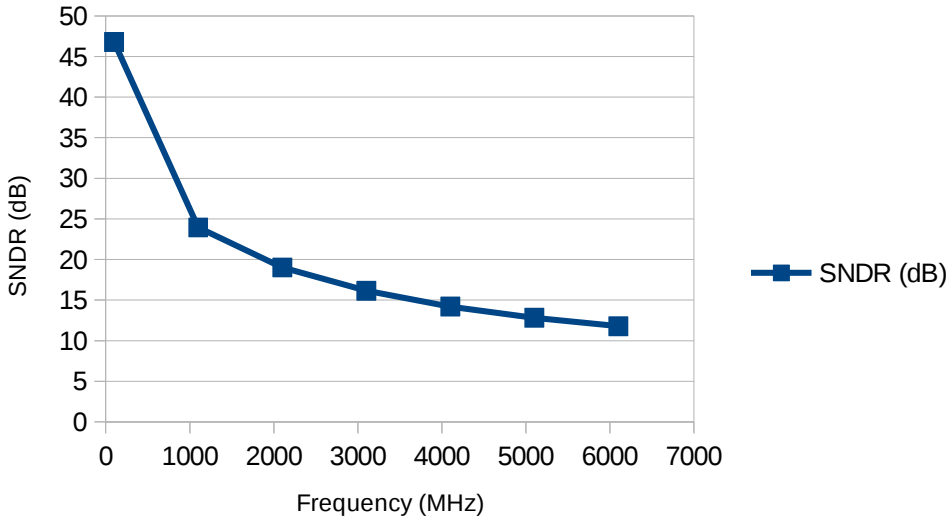

Figure 3b2: SNDR vs. input frequency

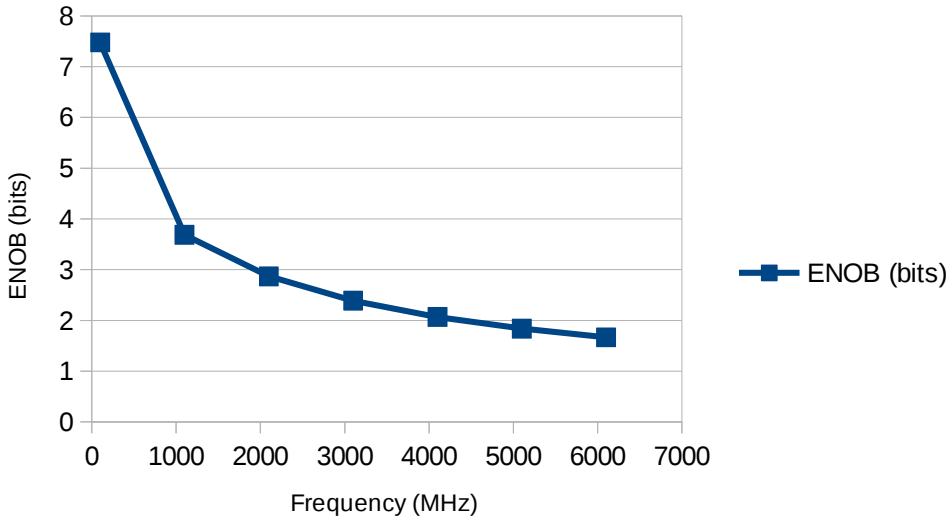

Figure 3b3: ENOB vs. input frequency