6-bit Segmented Current-Mode DAC Simulation and Design

2a. 6 bit binary-weighted current-mode DAC design

The design for the current-mode binary weighted DAC was carried out in the following stages. First, a high-level ideal system with each bit-controlled binary-scaled current source branch was outlined – here from the MSB branch to the LSB branch, the current is divided by half at every subsequent branch until the LSB branch (with current at I/32). Now, given our DAC reference voltage of 256mV, we can find the DAC output voltage due to only the MSB active which given our 50Ω output resistor gives us the current through the MSB branch, which is equal to our reference current (given an "ideal" Opamp):

$$V_{MSB} = \frac{32}{2^N} x\, V_{Ref} = \frac{32}{64} x 256\,mV = 128\,mV \quad \text{and hence}$$

$$I_{MSB} = I_{ref} = V_{MSB} / R_{out} = 128\,mV / 50\Omega = 2.56\,mA$$

Having a measure of our desired current, we can now design our current reference. First we can compute our reference resistor (assuming an ideal Opamp) which enforces Vref=256mV across Rref, therefore: $R_{ref} = V_{ref} / I_{ref} = 256\,mV / 2.56\,mA = 100\Omega$

Now, we can implement our reference resistor with 2 unsilicided P+ poly resistors in parallel with the following dimensions

$R_{width} = 2\mu m$ $R_{length} = 0.6\mu m$ $R_{unit} = 198.21\Omega$

with two devices in parallel (Nb =2): $R_{ref} = 99.1\Omega$

And we can implement our output resistor with 4 unit resistors in parallel (Nb=4) for a total output resistor: $R_{out} = 49.55\Omega$

Then, we proceeded to size the transistors to implement our current reference. Ideally we want the current reference switches to carry the same current as our MSB branch, this will also be 32 times the current for our LSB. Hence, we want the MSB current mirror to be sized equally to our reference and 32 times the size of the LSB current mirror, using the minimum dimensions for the kit as a starting reference: At first, for Q_ref = Q_MSB_mirror (2.5V devices): $L = 0.28\mu m$ $W_{total} = W_{f\_min} x 32 = 4\mu x 32 = 128\mu m$ $N_f = 32$ and for Q_bit = Q_cascode devices (1.1V devices): $L = 60\,nm$ $W_{total} = W_{f\_min} x 32 = 1\mu x 32 = 32\mu m$ $N_f = 32$

Now we need to make sure our GP 1.1V transistors meet the max current density limitations (at a bias and input voltage of 0.5V), i.e. given: $J = 0.05\,mA$ and $I_{ref} = 2.56\,mA$ Therefore, $w_{min} \geq 51.2\mu m$ Thus, we need to re-size our our cascode 1.1V devices, in our case Q_bit = Q_cascode becomes: $L = 60\,nm$ $W_{total} = W_{f\_min} x 64 = 64\mu m$ $N_f = 64$

Additionally, because the Opamp used in our reference is not ideal (leads to larger reference current), we would need to reduce our MSB mirror devices to generate 128mV at Vout under MSB active only: this would lead to the LSB mirror being smaller than our minimum dimensions, thus we increase the size of reference and MSB devices, Q_ref = Q_MSB_mirror: $L = 0.28\mu m$ $W_{total} = W_{f\_min} x 64 = 4\mu x 64 = 256\mu m$ $N_f = 64$

At this point we built and simulated the DC operating point of our reference and MSB branches alone (max voltage for Q_cascode and Q_bit was around 900mV and less and than 1.2V max supply for GP devices). Then, for each subsequent binary-scaled branch we halved the width and number of fingers for its Q_mirror, Q_bit and Q_cascode devices. Now, because the reference current is larger than our desired values for our MSB (due to Opamp finite gain, mentioned above) and subsequent branches, we need to fine-tune the widths of our mirrors (there are better ways of doing this: explored in next section): $W_{b5\_mirror} = 249.2\mu$ $W_{b4\_mirror} = 124.8\mu$ $W_{b3\_mirror} = 62.73\mu$ $W_{b2\_mirror} = 31.67\mu$ $W_{b1\_mirror} = 16.1\mu$ $W_{b0\_mirror} = 8.25\mu$ (based on testing the DAC output voltage for one binary bit at a time and comparing the result with our ideal values).

Finally we set up our Vpulse sources as noted in the write-up with twice the frequency from LSB to MSB clock inputs to test the transient output of our DAC (See figures 2a1 and 2a2 for the full schematic and DAC transient output voltage ramp). Here as is common with binary-weighted DAC architectures the dimensions spread for our switches is large, and there are prominent glitches at MSBs transitions as expected (proportionally noticeable at Vout/2, Vout/4 and Vout/8 corresponding to the transitions of b5, b4 and b3 respectively).

2b. INL and DNL Measurements

To calculate the input non-linearity: the non-linear deviation from the ideal DAC curve (i.e. after removing gain and offset errors) for every digital input code we can calculate:

$$V_{ideal\_step\_size} = V_{LSB} = \frac{V_{full\_scale}}{number\ of\ steps} = \frac{V_{full\_scale}}{2^N - 1} = \frac{V_{ref}\, x\, 63/64}{63} = \frac{252\,mV}{63} = 4\,mV$$

$$INL(LSB) = \frac{\text{current step size} - \text{ideal step size}}{\text{ideal step size}} = \frac{V_{step} - V_{LSB}}{V_{LSB}}$$

translated into pseudo-code:

$$INL(LSB) = \frac{(Vout[\text{next\_digital\_code}] - Vout[\text{current\_digital\_code}]) - V_{LSB}}{V_{LSB}}$$

We used a modified version of the dac_inl_8bits measurement cell in the ahdl library (copied cell to own library, modified Verilog-a source to support 6 bits, fixed deprecated function calls, enabled write to tsv file) that implements this function. This measurement cell was enabled to either write the measured INL for every code, or the maximum INL and respective digital code for each transient run, all the data was post-processed with spreadsheet software for plotting. See figure 2b1 for measured INL for a single transient response at 65C nominal corners, see figures 2b2 and 2b3 for the 50 monte-carlo runs simulating process variation and device miss-match at 65C, both DAC output voltages and maximum INL (at digital code) per run respectively. The DNL is the difference in units of LSBs between adjacent DAC output step values from the ideal 1LSB step size at every digital code, or alternatively simply the difference between INL measurements at every digital code. For the DNL measurement we used the dac_dnl_8bits measurement cell modified as before (for ease of exporting the computed data for Monte-carlo runs). See figure 2b4 for the measured DNL for a single transient response at 65C and figure 2b5 for the maximum DNL (at digital code) per Monte-carlo run respectively. Here as before we see the non-linearity errors are largest at MSBs transitions due to glitches natural to binary-scaled DAC architectures.

2c. SDR and ENOB Measurements

Here as recommended in the write-up, the ideal 8-bit ADC (only 6 output bits used) was used to digitize an input sinusoid of varying test frequencies (first with an ADC clock of 10Gs/s and then with 15Gs/s) (see figure 2c1 for DFT measurement setup at 100MHz), then following a similar approach from assignment 4, the SDR was computed and subsequently the effective number of bits were computed at each frequency: $ENOB = N_{eff} = (SDR - 1.76)/6.02$ (See figures 2c1, 2c2, 2c3 and 2c4 for the SDR and ENOB vs frequency at both sampling rates). Finally the effective resolution

bandwidth was computed (reference textbook, page 618): the bandwidth over which a converter's peak SDR is within 3dB of its best value or equivalently the bandwidth over which the ENOB (Neff) is within 0.5 bits of its peak value. In our case, we computed the slope from the first two low frequency points and calculated the frequency were the ENOB FoM dropped by 0.5 bits from its highest value, mainly: $402.847\,MHz$ and $384.738\,MHz$ or approximately $BW_{eff} \sim 400\,MHz$.

3a. 6 bit segmented current-mode DAC design

For the design of the differential segmented current-mode DAC for this section (with specs: 3 segmented MSBs, 200mV full scale and 15Gs/s sampling rate), a similar design flow was followed from the previous section with a few important differences. For the thermometer coded section of the DAC, given 3 segmented bits, we need $2^N - 1$ branches, or 7 thermometer coded current-mode branches. Additionally the topology of each of our branches changed slightly as both GP 1.1V input switches were now driven by complementary clocks with differential outputs each to it's respective shared output load resistor (2 output resistors, each for each differential output voltages from all branches). Next a system level diagram (using both thermometer-code-controlled and bit-controlled ideal current sources) was used to understand the magnitude of the currents for each equal thermometer coded branch and each binary-scaled branch. In our case, we know each thermometer code branch (only active by itself) is equivalent to digital code b'=1000 or 8, therefore if only one of the thermometer-coded branches is active (and they are all the same), we should see at the output: $V_{out} = 8/63\,x\,V_{ref} = 25\,mV$ From this output voltage and given our $50\,\Omega$ output resistor we can determine both the thermometer coded current for each equal branch and our reference "ideal" current, mainly:

$I_{ref} = 25\,mV / R_{out} = 25\,mV / 50\,\Omega = 500\,\mu A$ and we can determine our reference resistor as before:

$R_{ref} = V_{ref} / I_{ref} = 200\,mV / 500\,\mu A = 400\,\Omega$

And we implemented our reference resistor using an unsilicided P+ Poly resistor with: $R_{width} = 2\,\mu m$, $R_{length} = 1.16\,\mu m$ for a unit and reference resistance of $R_{unit} = R_{ref} = 400.86\,\Omega$. Our output load resistors were then implemented as 8 unit resistors in parallel (Nb = 8) for a total of: $R_{out} = 50.11\,\Omega$.

Subsequently we chose the sizes for our our PMOS transistors: here we want the current reference transistors to carry the same current as our thermometer coded branches transistors, this will be 8 times the current for our LSB binary branch, or 8 times the size of our LSB switches. Then, once again starting from minimum dimensions as a reference, we came up with good first starting values, At first, for Q_ref = Q_t-coded_mirrors (2.5V devices): $L = 0.28\,\mu m$

$W_{total} = W_{f\_min}\,x\,8 = 32\,\mu m \qquad N_f = 8$

At first, for Q_bias = Q_t-coded_bit (1.1V devices): $L = 60\,nm$

$W_{total} = W_{f\_min}\,x\,8 = 8\,\mu m \qquad N_f = 8$

Then scaling our transistors for the reasons outlined in the previous section (i.e. to meet max current density for GP devices and stay above minimum dimensions for 2.5V LSB devices):

Q_bias = Q_t-coded_bit becomes: $L = 60\,nm$

$W_{total} = W_{f\_min}\,x\,16 = 16\,\mu m \qquad N_f = 16$

Q_ref = Q_t-coded_mirrors (2.5V devices): $L = 0.28\,\mu m$

$W_{total} = W_{f\_min}\,x\,16 = 64\,\mu m \qquad N_f = 16$

Hence, we have all the transistors' dimensions for our reference and all equal thermometer coded branches. Then for the remaining binary branches (i.e. from b2, b1 to b0) the dimensions of our transistors will be scaled by half for each successive branch as before. Finally to fine-tune the widths of our mirror transistors to the precise branch current and output voltage (with only one bit, or T-code line active at a time), we followed a different approach, we simply increased the size of the relative PMOS transistor for our reference, while keeping all other mirrors in our DAC sized almost perfectly with the dimensions above (more optimally we could have used multiple identical devices in parallel). The final dimensions are

$W_{ref} = 70.44\,\mu \qquad W_{t\text{-}coded\_mirrors} = 64\,\mu \qquad W_{b2\_mirror} = 32.1\,\mu$

$W_{b1\_mirror} = 16.26\,\mu \qquad W_{b2\_mirror} = 31.67\,\mu$

Now it was necessary to implement the 3 to 7 binary to thermometer code encoder. For this purpose a spreadsheet was used to describe the truth table to be able to come up with the boolean logic expressions for each thermometer coded line:

$d_0 = b_2 + b_1 + b_0 \qquad d_1 = b_2 + b_1 \qquad d_2 = b_1 b_0 + b_2 \qquad d_3 = b_2$

$d_4 = b_2 (b_1 + b_0) \qquad d_5 = b_2 b_1 \qquad d_6 = b_2 b_1 b_0$

At this point the 6 bit segmented current-mode differential DAC was designed and its output could be plotted for correct operation. See figures 2a1, 2a2 and 2a3 for the full schematic, encoder cell and dc operating points of reference and T-coded cell (all voltages are below 1.2V for GP transistors as required), see figure 2a4 for binary and thermometer code clock signals and reference DAC output ramp.

3b. INL and DNL Measurements

The INL and DNL measurements were obtained exactly as before (see process on previous section) both for a single nominal measurement (See figures 3b1 and 3b2 for INL and DNL respectively**)** and over 50 monte-carlo runs for each measurement (see figures 3b3 and 3b4 for max INL and DNL for each run respectively). Here there are a couple of remarks worth making: First in the time domain, we no longer see the very large proportional well-defined glitches at the MSB transitions from before (we also see the max INL and DNL errors more clearly distributed around different digital codes), also the overall magnitude of the INL errors has decreased. Unfortunately however ,we now we see spikes due to the remaining transitions of the binary scaled LSBs but more importantly due to clock feed-through. This is because when we changed the architecture of the circuit from single-ended to differential, we removed the cascode transistor biased at 0.5V, the roles of this transistor are many-fold, first to isolate/protect our current mirror drain from fluctuations at the output but more importantly in this case to guard against clock feed-through from the input transistor, additionally the complementary clocks represent themselves as differential feed-through signals at the output and do not benefit from common-mode rejection.

3c. SDR and ENOB Measurements

Here the exact same procedure was used as before but now with a single ADC clock of 15Gs/s at the slightly different input tone frequencies (see figure 3c1 for DFT measurement setup at 100MHz). Subsequently the SDR and ENOB was computed at each frequency and plotted using spreadsheet software (See figures 2c2, 2c3). Finally the effective resolution bandwidth was calculated from the plot as before to be $583.559\,MHz$ or approximately $BW_{eff} \sim 600\,MHz$.

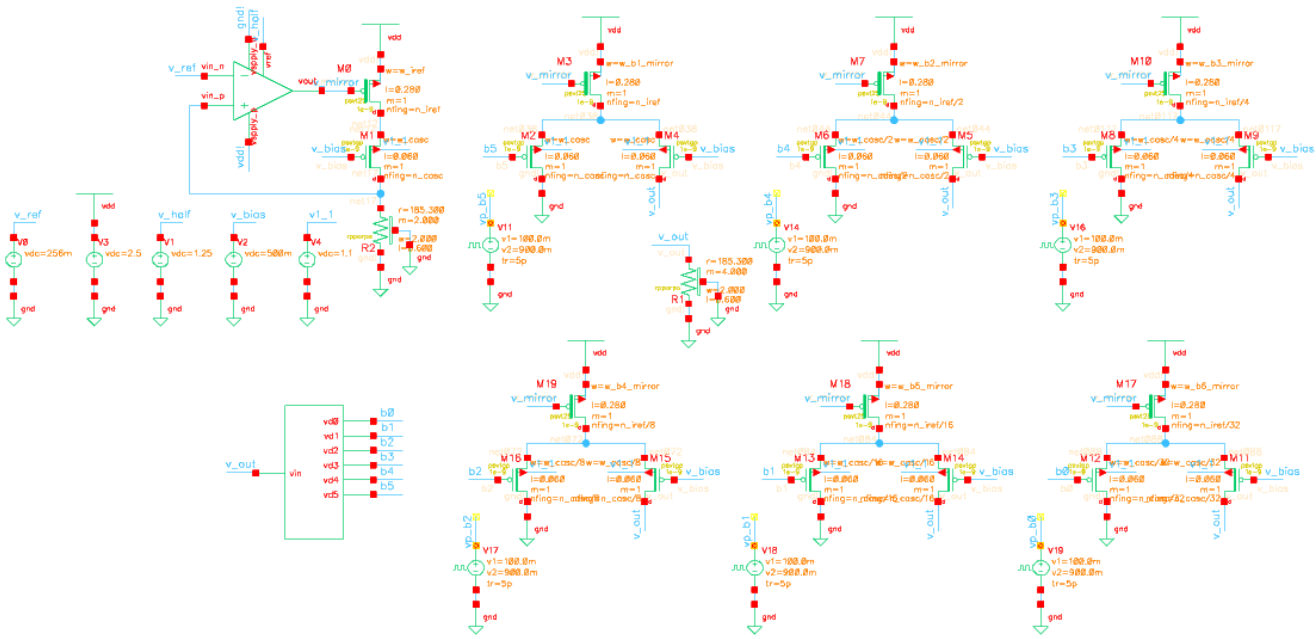

Figure 2a1: 6b binary-weighted DAC full schematic (here bit inputs driven from measurement block not pulse sources)

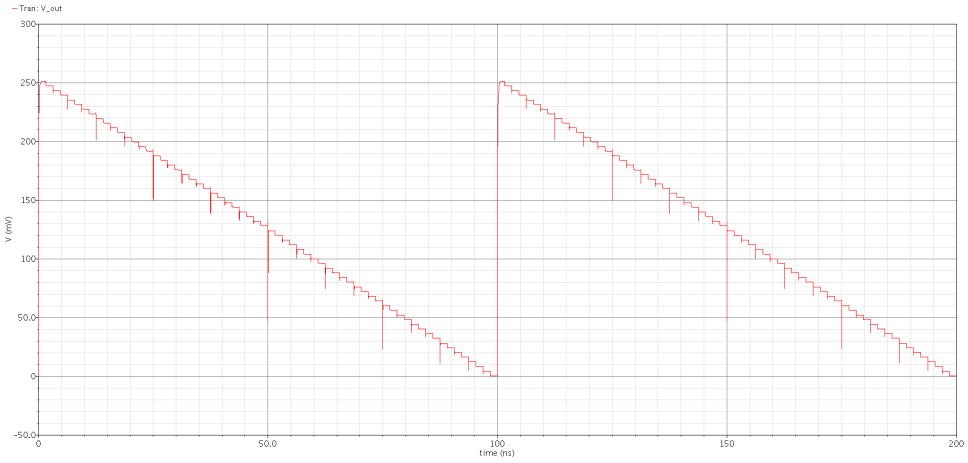

Figure 2a2: 6b binary-weighted DAC Output (here bit inputs driven from pulse sources at 50% duty cycle)

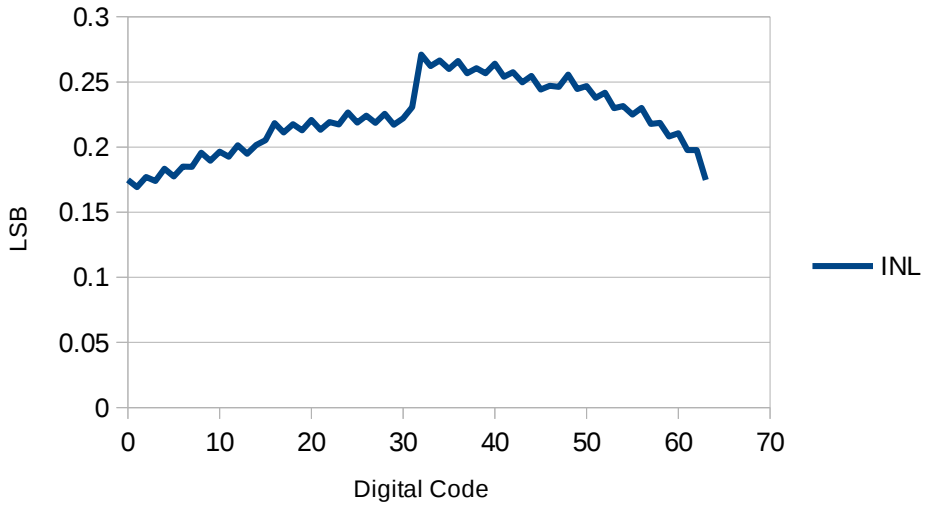

Figure 2b1: measured INL for a single transient response at 65C (nominal corners)

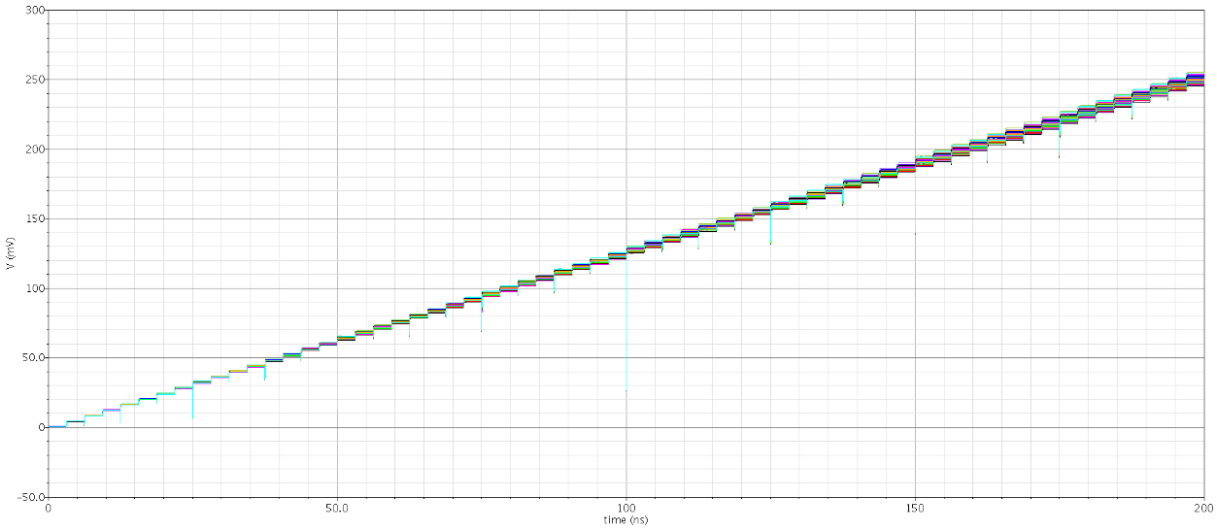

Figure 2b2: Monte-carlo runs simulating process variation and device miss-match at 65C

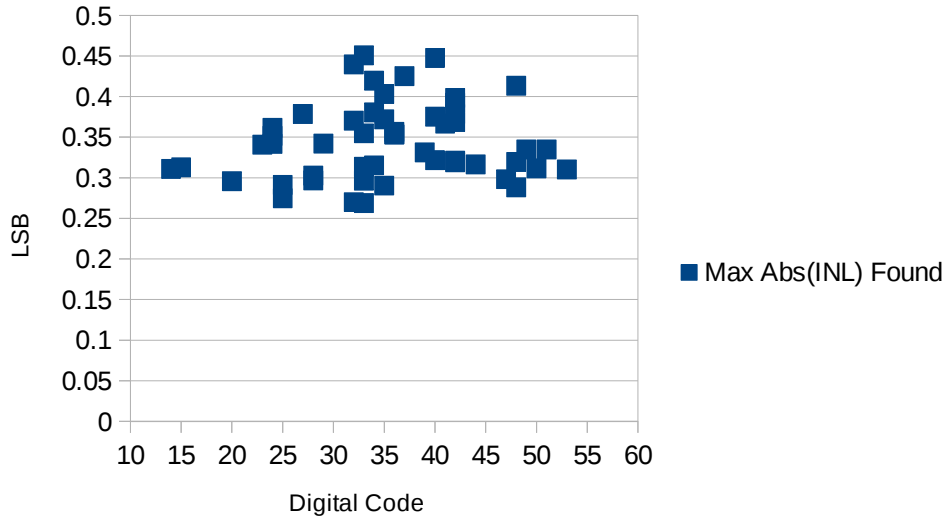

Figure 2b3: Maximum Abs(INL) (at digital code) per Monte-carlo run (each data point)

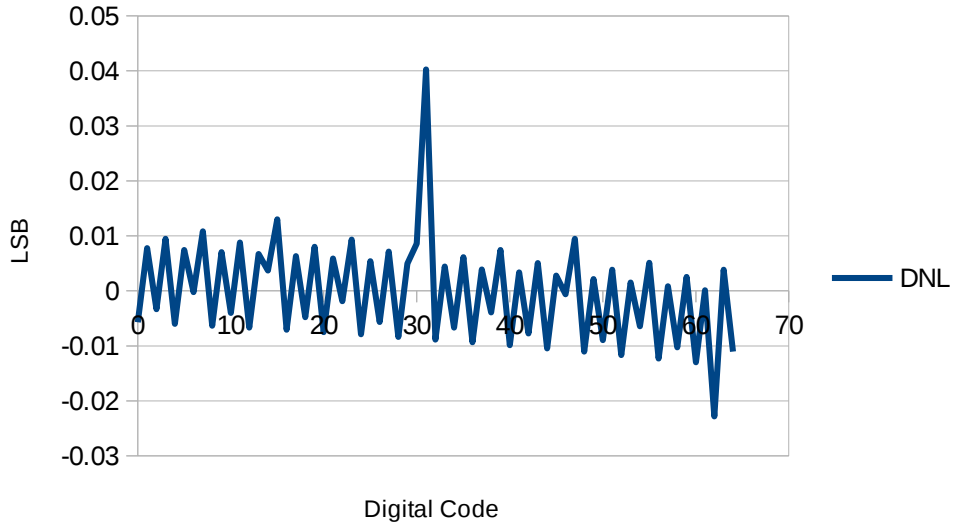

Figure 2b4: Measured DNL for a single transient response at 65C

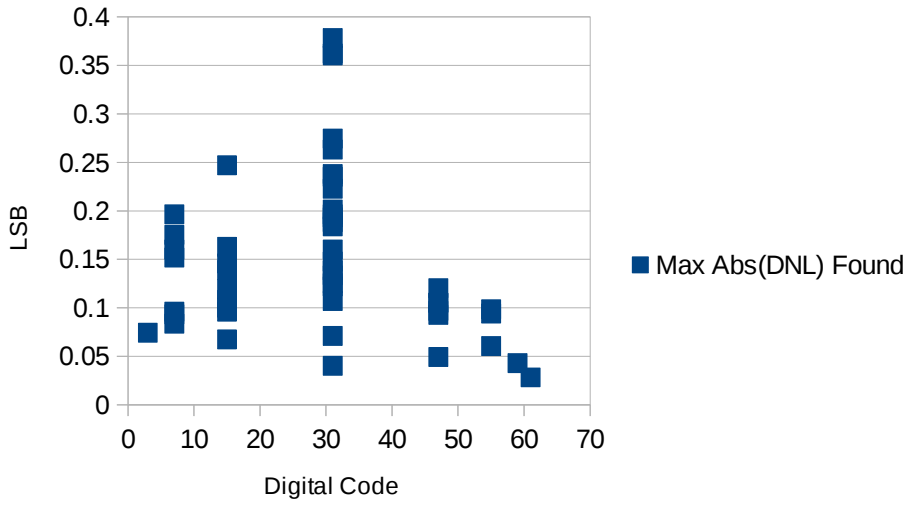

Figure 2b5: Maximum Abs(DNL) (at digital code) per Monte-carlo run (each data point)

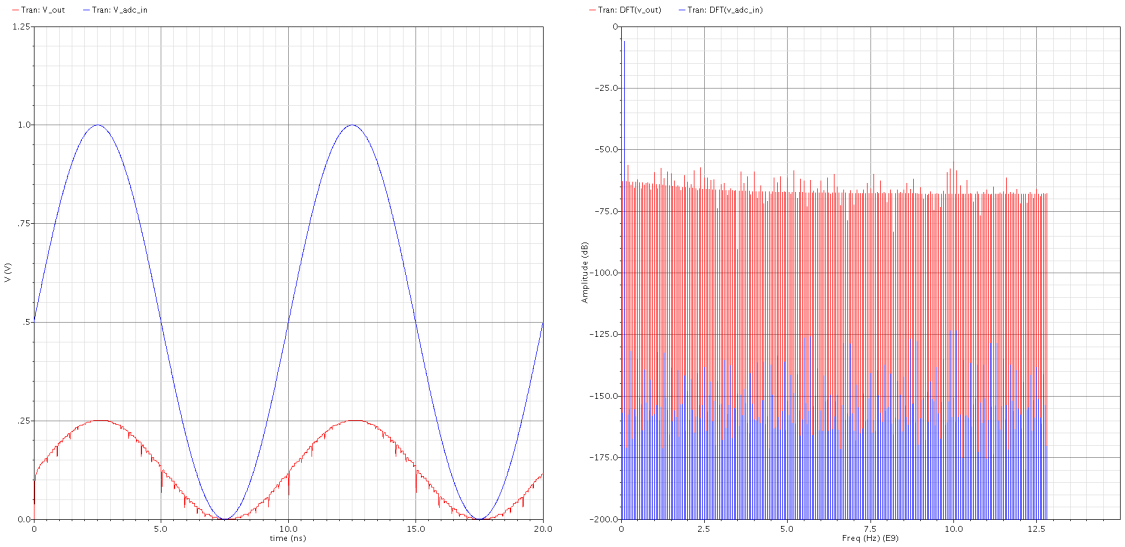

Figure 2c1: DFT setup for SDR measurements (test tone at 100MHz)

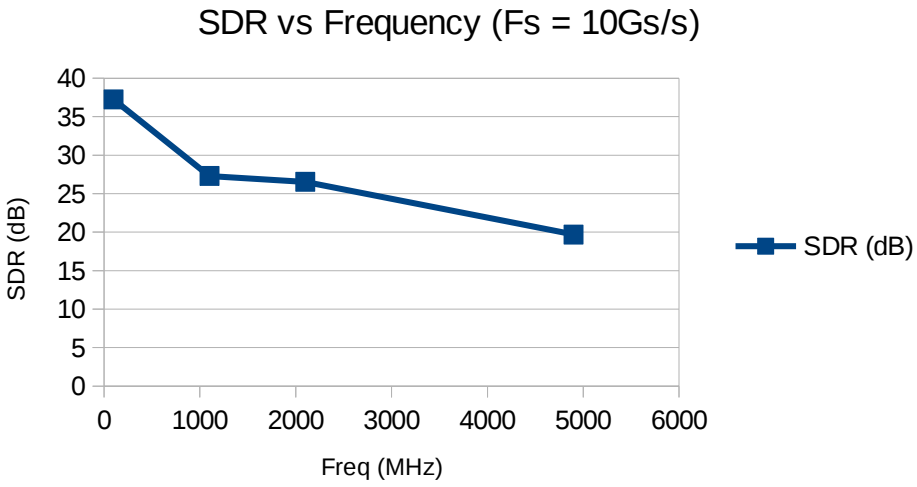

Figure 2c2: SDR vs. Frequency (at Fs = 10Gs/s)

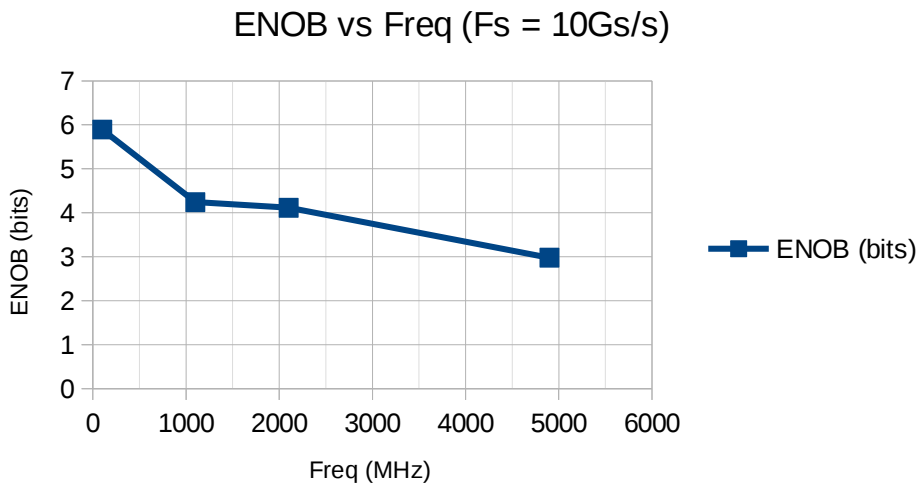

Figure 2c3: ENOB vs. Frequency (at Fs = 10Gs/s)

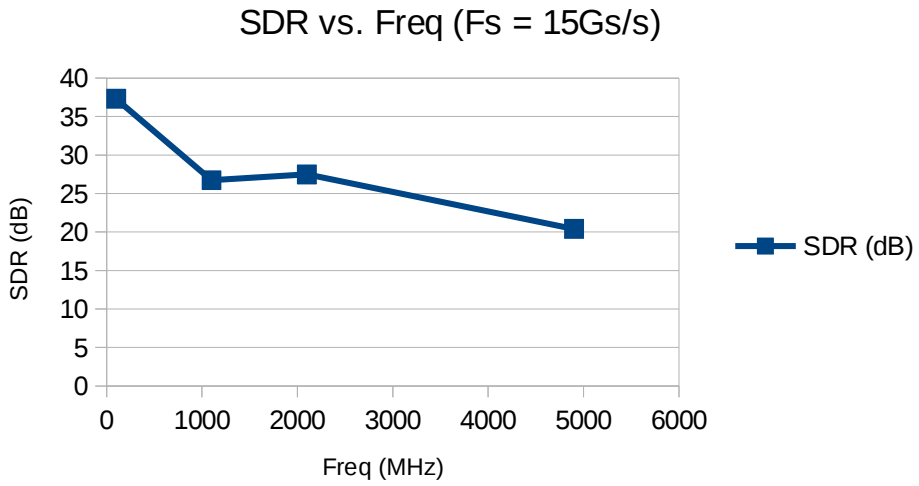

Figure 2c4: SDR vs. Frequency (at Fs = 15Gs/s)

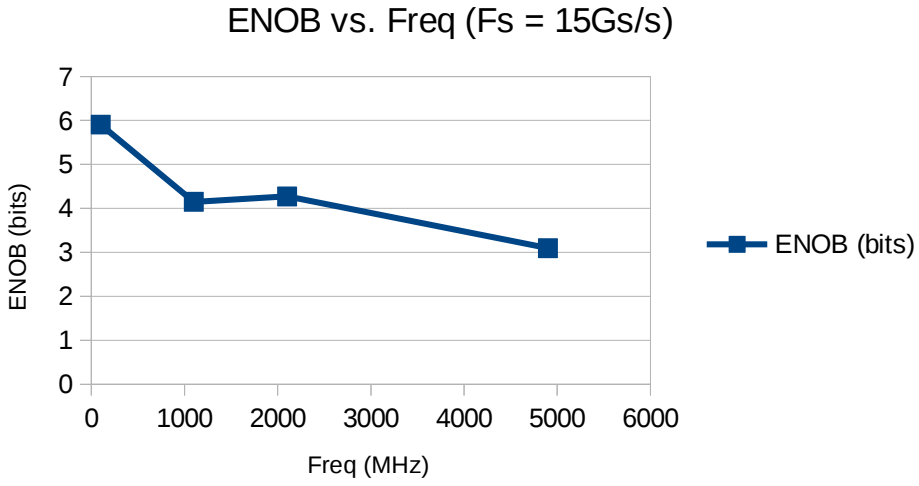

Figure 2c5: ENOB vs. Frequency (at Fs = 15Gs/s)

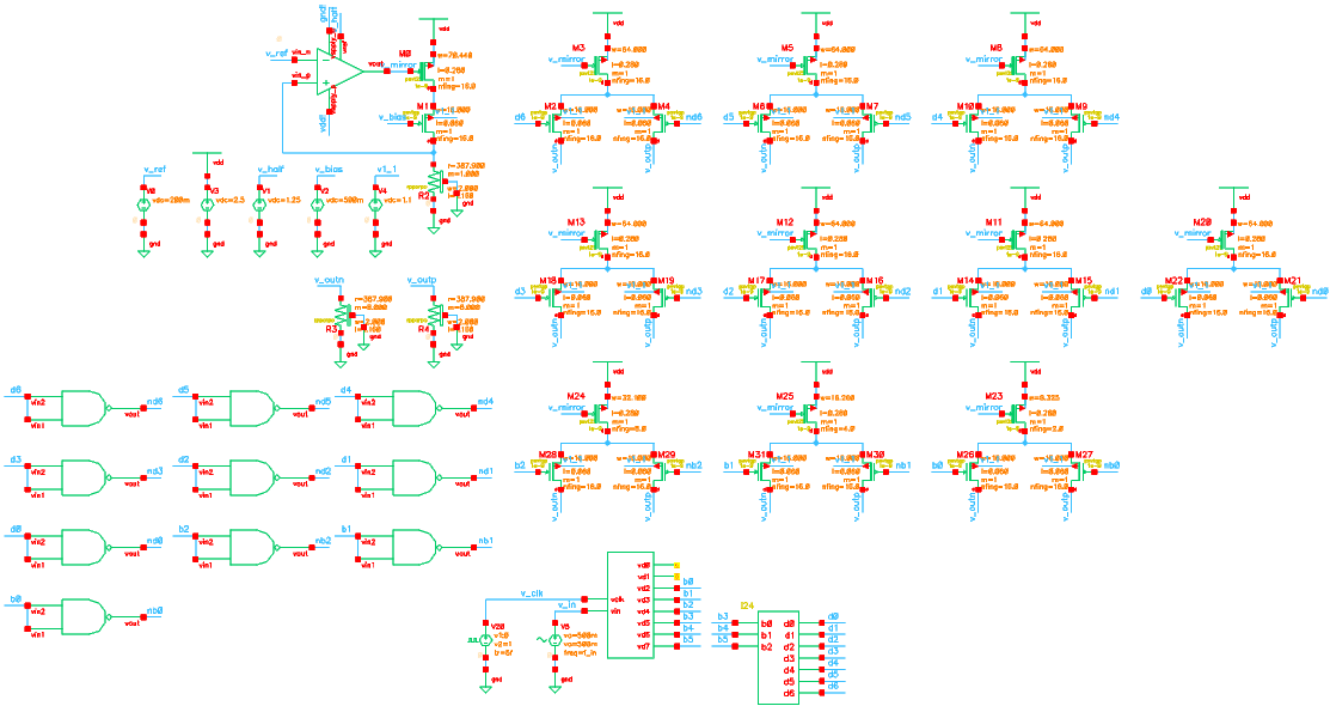

Figure 2b1: 6b segmented differential DAC full schematic

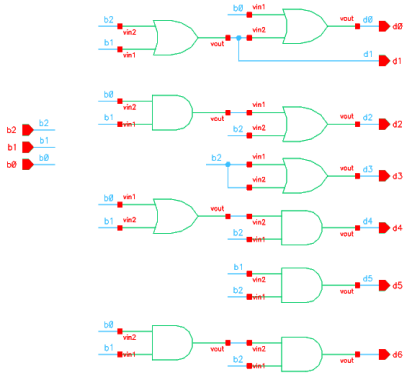

Figure 2a2: 3 to 7 binary to thermometer code encoder cell

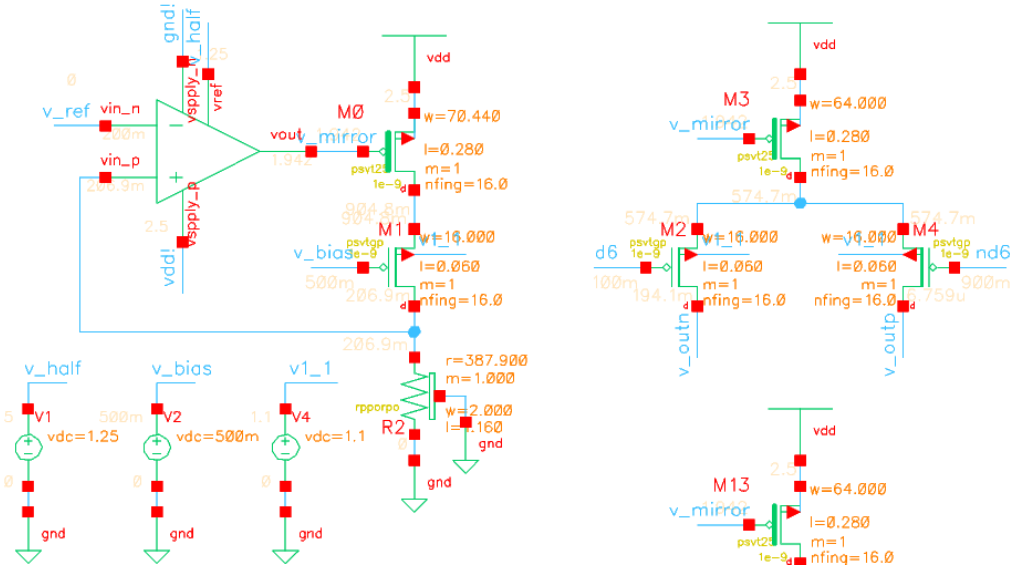

Figure 2a3: Close-up of current reference and T-coded cell (bit unactive) for DC op points (all GP devices < 1.2V)

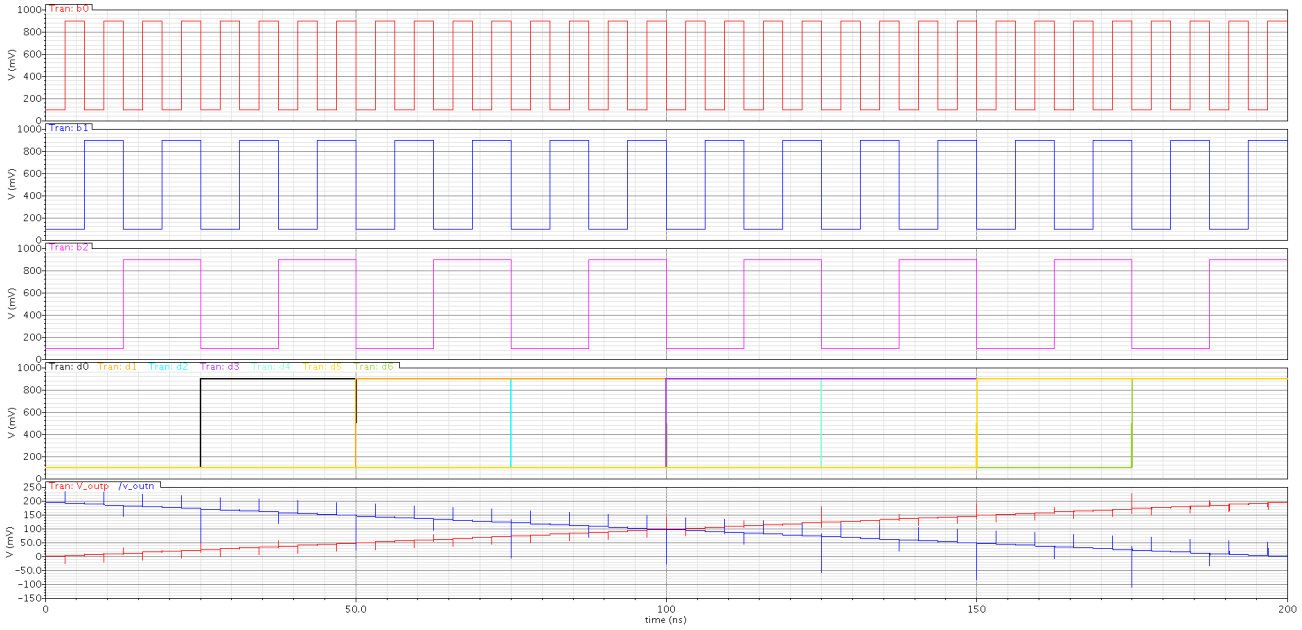

Figure 2a4: Binary and thermometer-code clock signals and reference output ramp (see clock feed-through errors)

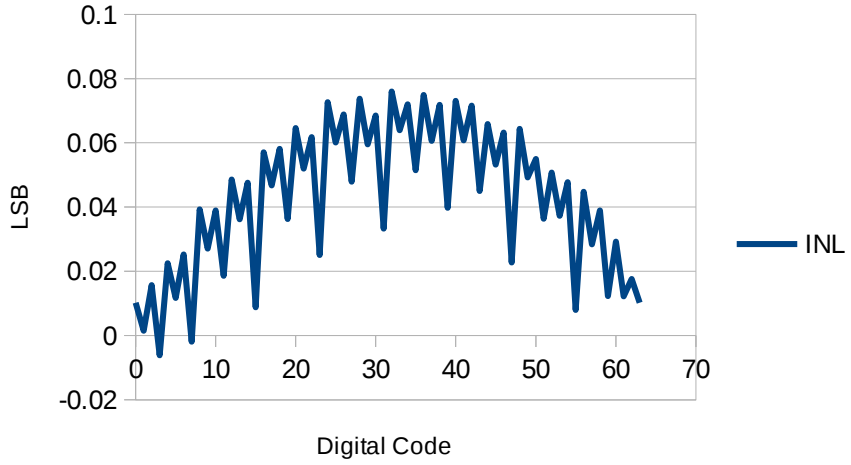

Figure 3b1: Measured INL for a single transient response at 65C (nominal corners); see decreased INL magnitude.

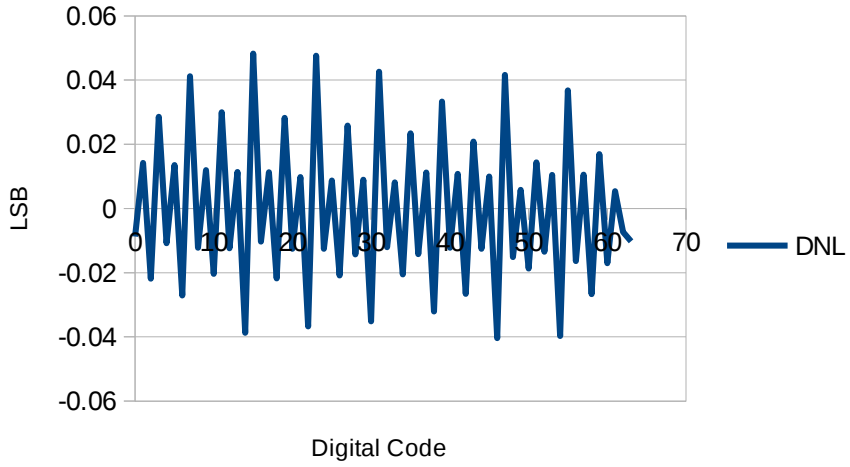

Figure 3b2: Measured DNL for a single transient response at 65C

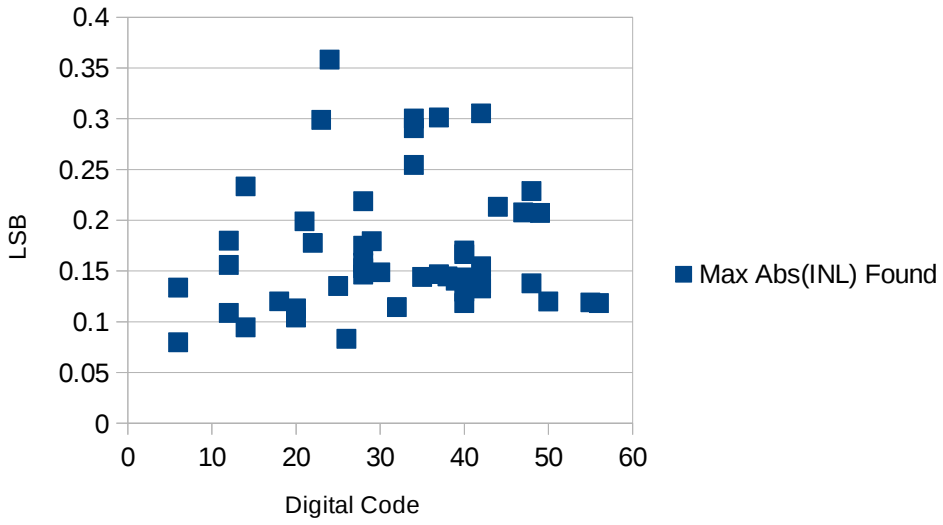

Figure 3b3: Maximum Abs(INL) (at digital code) per Monte-carlo run; notice larger spread across many digital codes.

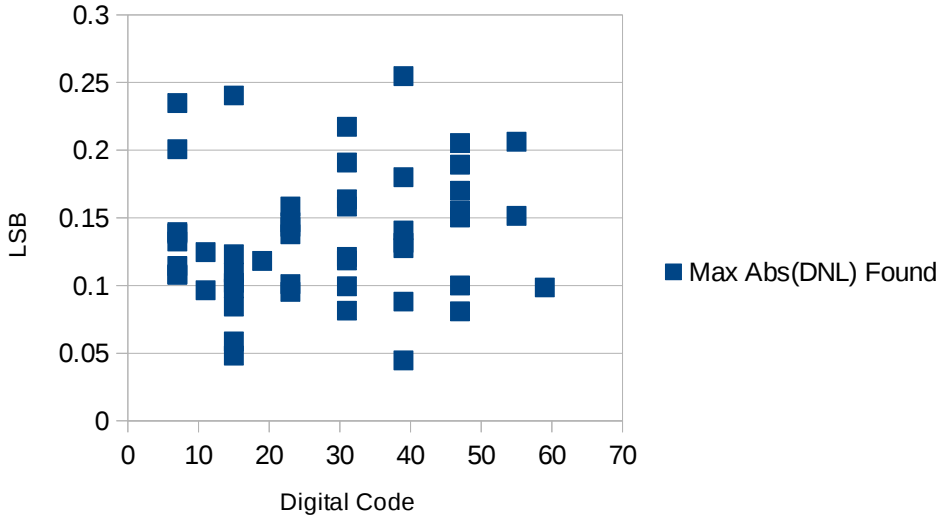

Figure 3b4: Maximum Abs(DNL) (at digital code) per Monte-carlo run; max errors now across different bit transitions

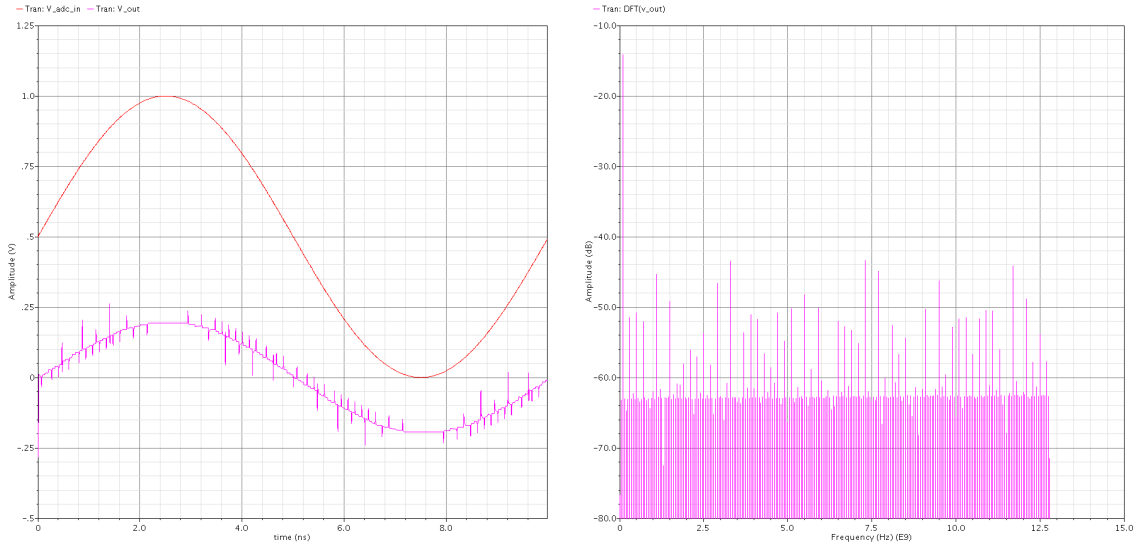

Figure 3c1: DFT setup for SDR measurements (test tone at 100MHz)

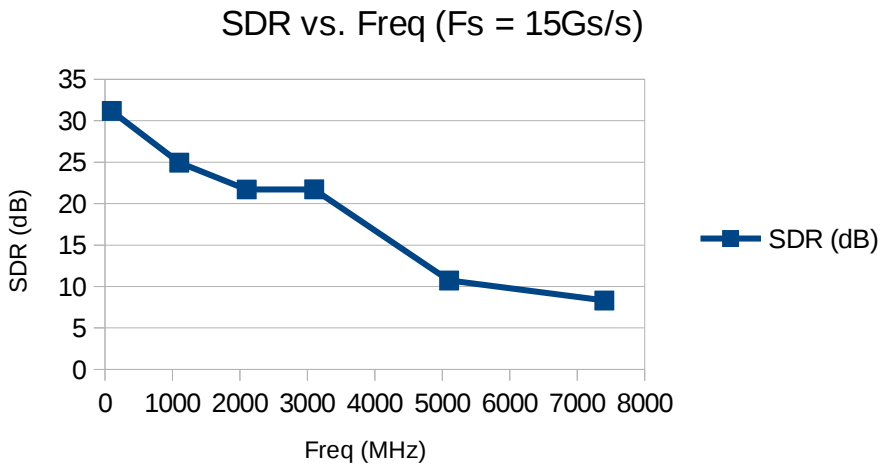

Figure 3c2: SDR vs. Frequency (at Fs = 15Gs/s)

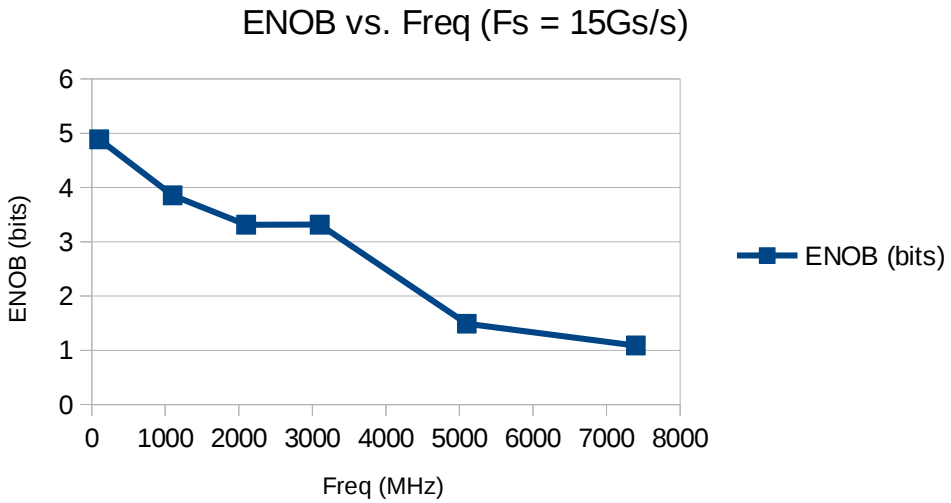

Figure 3c3: ENOB vs. Frequency (at Fs = 15Gs/s)