CMOS Sample and Hold Circuit Simulation and Design

2. CMOS T/H and S/H simulation:

First, the CMOS S/H test-bench was built with the required components as noted in the write-up, next the clock pulse signal-source parameters were chosen (non-overlapping 2GHz clocks with 25% duty cycle and 5pS rise and fall times), finally the component parameters were chosen appropriately following the assignment guidelines.

2a. 3dB bandwidth AC response of S/H circuit

First all switches were put in the ON condition in order to allow for the AC bandwidth measurement. Then the AC magnitude transfer function was measured at the S/H and T/H nodes vs input and plotted in a dB scale (see figure 2a), as seen from the plot:

$$f_{\text{th\_3db}} = 11.96\,GHz \qquad f_{\text{sh\_3db}} = 7.722\,GHz$$

Compared to our previous assignment, as we are using larger transistors (twice as wide), this has two counter-acting effects: first, the ON resistance of our switches will decrease (this will act to increase the bandwidth of our switches), on the other hand (and detrimentally to our performance) the parasitic capacitances of our transistors will increase with increased width. Some of this capacitance adds to our hold capacitance and reduces our bandwidth (by the RC combination of our switches and hold capacitors; these capacitors were not present in assignment 3 section 2), additionally larger parasitic capacitances lead to greater charge injection and clock feed-through errors. In the case of our S/H circuit, and as will be seen in later simulations, the decrease in ON resistance leads to bandwidth gains for our S/H response but worse noise performance.

2b. Transient response of S/H circuit (500mVpeak amplitude)

To measure the transient response of our circuit, first the clocks were re-enabled to drive our CMOS switches as required, subsequently a 50MHz 500mVpeak sinusoidal input signal was applied to our circuit and the transient response was measured at the input, T/H and S/H outputs (see figure 2b1). From our plot we can see that the sampling pedestal or hold steps (error that occurs each time a sample and hold goes from sampling mode to hold mode) which are due to charge injection are worse at the high and low swings of our waveform, this is a common problem with the use of CMOS transmission gates. At the center of our waveform, the charge injection due to NMOS and PMOS transistors largely cancels out as both transistors are operating symmetrically (ON) and the charge injected is equal but opposite. However at the upper swing only the PMOS is operating fully ON while the NMOS is OFF, therefore the positive charge injection by the PMOS transistor dominates and produces a resultant positive hold step. (this can be clearly seen for our upper swing in figure 2b2). An equal but opposite in polarity effect is present at the lower swing of our waveform due to only our NMOS transistors operating fully ON. It is this “signal-dependent” sampling pedestal or step which introduces non-linear distortion harmonics. In our case the sampling pedestal values at the high and low swing of our waveforms (worst-case) are:

$$V_{\text{step\_error, high}} = 5.2\,mV \qquad V_{\text{step\_error, low}} = -7.96\,mV$$

Next, we are asked to simulate the frequency spectrum at the input and output node (see figure 2b3 for the superimposed FFT for clarity). The SFDR of our response (using the magnitude of our fundamental minus largest harmonic):

$$SFDR = -19.8 + 40.81\,dB = 40.81\,dB$$

As noted before, the cause of the non-linearity (harmonics distortion seen in spectrum) is due to the signal-dependent charge injection errors which generate the sampling pedestals only found at the high and low ends of our waveform.

2c. Transient response of S/H circuit (5mVpeak amplitude)

Here, the same S/H test-bench was used as before, but now the input signal amplitude was reduced to 5mVpeak. Then the transient response of the circuit was measured at the input, T/H and S/H outputs (see figure 2c1). In this case because our signal amplitude is small, it stays close to our reference mid voltage where both transistors are operating symmetrically ON. It is important to note that we still see both clock-feedthrough errors (high frequency spikes) and charge injection errors (sampling pedestal/hold steps) (see figure 2c2) but here they are constant and signal-independent, this translates to broadband noise added to our inherent noise floor as opposed harmonics distortion I.e. non-linearity as seen before. In addition note that while we see the magnitude of our transient response errors being greater, this is only relative to our small input signal (our clock parameters and switch dimensions have remained the same). For our small input amplitude, looking at our sampling pedestal values at the high and low swings of our waveforms we find:

$$V_{\text{step\_error, high}} = 1.549\,mV \qquad V_{\text{step\_error, low}} = -1.79\,mV$$

Subsequently, we plot the DFT of our transient response at input and output nodes of our circuits (see figure 2c3). As noted before because we no longer have signal-dependent charge injection, we no longer have non-linear distortion harmonics. In other words, by decreasing the input amplitude of our signal, we have improved the linearity of our response, but unfortunately as we decrease our input signal amplitude, we can now see our response is noise-limited. Thus, as our response is noise-limited and we no longer have non-linear harmonics and a better measure of performance is SNR: $SNR = -58.52\,dB + 70.1\,dB = 11.58\,dB$

2d. Input-intercept point: IIP3

Considering first the case with 500mVpeak input amplitude, we compute our OIP3 first: $OIP3 = I_{D1} - ID_3/2$

$$OIP3 = -19.8\,dB + 20.40\,dB = 0.605\,dB$$

and because our S/H has 0dB of gain, mapping to our input:

$$IIP3 = OIP3 - 0\,dB = 0.605\,dB \quad \text{or in dBm} \quad IIP3 = 0.605\,dB$$

Now considering the case with 5mVpeak input amplitude, we have: $OIP3 = -52.73\,dB \qquad IIP3 = -52.73\,dB$

2e. SFDR (function of frequency) and large-signal bandwidth

Next we are asked to plot the changes in the SFDR of our response (with an amplitude of 500mVpeak) as a function of frequency. Here we are sweeping a frequency range of 50 – 950MHz (below Fs/2) in 100MHz frequency steps and obtaining our SFDR values by hand from individual successive transient (DFT) simulations, finally we collect all of our values and plot them using spreadsheet software (see figure 2e1). Having looked at the transient simulation in time and DFT side by side at each frequency step, there are a couple of things worth mentioning: First at frequencies below or equal to 250MHz we have a clearly distinguishable fundamental with the present non-linear harmonics at higher frequencies (but below FS/2) as expected, at frequencies above

250MHz we start seeing some aliasing due to harmonics lying beyond Fs/2, then at frequencies beyond 550MHz aliasing becomes more prominent and we start seeing aliased frequencies at lower frequencies than our fundamental, finally beyond 750MHz the aliased lower frequency components become greater than our fundamental and our measured SFDR is no longer representative. From our simulated SFDR points vs frequency it is difficult to come up with a definite figure for the large signal bandwidth measure: the majority of points taken decrease in SFDR by more than 3dB between consecutive points.

3. 4x Time-interleaved S/H ADC front-end

After reading both reference papers, and using the clock specification (Fclk = 8MHz), the direct sampling 4x interleaved front end was designed as follows. First, we focused on building a test-bench to understand only one interleaved channel (with the 4 sub-sampling switches)(see figure 3q1). Next we focused on determining the minimum size for our transmission gate transistors (to minimize parasitic capacitances: charge injection and clock feed-through errors) while still meeting the necessary bandwidth for our S/H single-channel front end (see figures 3q2a and 3q2b) for AC bandwidth measurement from input to Cs,adc with minimum dimension transistors, and 10um-wide 10-fingers transistors respectively). As we can see from our simulation, and for the reasons mentioned previously, larger transistors in general (with lower Ron) improve the bandwidth of our response – the speed or input frequency the circuit can handle – the price we pay however is larger charge-injection and clock feed-through errors. In our case, our required clock frequency is very modest, so we can choose the minimum dimension switches while still meeting our bandwidth requirement.

$f_{\text{ds\_3db}} = 285.6\,MHz \qquad f_{\text{ss\_3db}} = 443.6\,MHz$

Next we designed the clocking scheme on paper – critical component for time-interleaved ADC front-ends which can get complex for increasing number of channels – to make sure it agreed with our understanding of the paper, for our direct sampling switches, given: $F_{ds} = 8\,MHz \qquad T_{ds} = 125\,nS$ We chose:

$\phi_{\text{ds\_pulse\_duty\_cycle}} = 0.2\,xT_s = 25\,nS \qquad T_{rise} = T_{fall} = 5\,pS$ and,

$\phi_{\text{ds1\_delay}} = 0 \qquad \phi_{\text{ds2\_delay}} = 31.25\,nS \qquad \phi_{\text{ds3\_delay}} = 62.5\,nS$

$\phi_{\text{ds3\_delay}} = 93.75\,nS$

And for our sub-sampling switches, given:

$F_{ss} = F_{ds}/4 = 2\,MHz \qquad T_{ss} = 500\,nS$ We chose:

$\phi_{\text{ss\_pulse\_duty\_cycle}} = \phi_{\text{ds4\_end}} - \phi_{\text{ds2\_start}} = 87.47\,nS$ and our sub-sampling delay expressions (as a function of direct sampling parameters) for our first channel:

$\phi_{\text{ss11\_delay}} = \phi_{\text{ds2\_delay}} = 31.25\,nS \qquad \phi_{\text{ss12\_delay}} = \phi_{\text{ds2\_delay}} + T_{ds} = 156.25\,nS$
$\phi_{\text{ss13\_delay}} = \phi_{\text{ds2\_delay}} + 2\,T_{ds} = 281.25\,nS \qquad \phi_{\text{ss14\_delay}} = \phi_{\text{ds2\_delay}} + 3\,T_{ds} = 406.25\,nS$

For our second channel:

$\phi_{\text{ss21\_delay}} = \phi_{\text{ds3\_delay}} = 62.50\,nS \qquad \phi_{\text{ss22\_delay}} = \phi_{\text{ds3\_delay}} + T_{ds} = 187.5\,nS$
$\phi_{\text{ss23\_delay}} = \phi_{\text{ds3\_delay}} + 2\,T_{ds} = 312.5\,nS \qquad \phi_{\text{ss24\_delay}} = \phi_{\text{ds3\_delay}} + 3\,T_{ds} = 437.5\,nS$

For our third channel:

$\phi_{\text{ss21\_delay}} = \phi_{\text{ds3\_delay}} = 62.50\,nS \qquad \phi_{\text{ss32\_delay}} = \phi_{\text{ds4\_delay}} + T_{ds} = 218.75\,nS$
$\phi_{\text{ss33\_delay}} = \phi_{\text{ds4\_delay}} + 2\,T_{ds} = 343.75\,nS \qquad \phi_{\text{ss34\_delay}} = \phi_{\text{ds4\_delay}} + 3\,T_{ds} = 468.75\,nS$

and for our last fourth channel:

$\phi_{\text{ss41\_delay}} = 0 \qquad \phi_{\text{ss42\_delay}} = 125\,nS \qquad \phi_{\text{ss43\_delay}} = 250\,nS \qquad \phi_{\text{ss44\_delay}} = 375\,nS$

The clocking scheme for our direct sampling switches is as follows: Each direct sampling clock pulse is active for 20% of the total period Tds with the extra 5% in between phase pulses to allow for non-overlapping dead-time. The scheme for our sub-sampling switches (taking only the first channel as an example): right after the falling edge of the direct sampling pulse ϕ_{ds1}, our first sub-sampling switch ϕ_{ss11} is turned ON for the remaining duration of our direct-sampling period Tds, then ϕ_{ds1} is ON again and after the falling edge, ϕ_{ss12} is turned ON for the remaining duration of our direct-sampling period Tds, this pattern repeats for ϕ_{ss13} and ϕ_{ss14}; the same clocking scheme is used for the other channels and their respective sub-sampling switches but with different delays (from above).

The transient simulation and DFT for one channel at the input and output of discrete sampling and sub-sampling switches is provided (figure 3q3 and 3q4 respectively). We are using a reference input signal of 500mVpeak at 200KHz (the same input frequency to clock ratio of 0.025 from section 2). The SFDR at the output of the first channel, first sub-sampling switch:

$SFDR = -18.12 + 37.527\,dB = 19.407\,dB$

Next, to calculate the SFDR vs a range of frequencies (at the output of a single sub-sampling switch), we chose our frequency range to be 100KHz to 4MHz (Fs/2) in 400KHz frequency steps (but including our reference input at 200KHz) (see figure 3q5). Here we encountered the same problem as before: at most frequency points the reduction in SFDR is greater than 3dB, in addition aliasing is much worse in this case. This is because each sub-sampling switch is sampling the held signal once for every 4 clock pulses (Fs), therefore the maximum signal we can sample at each sub-sampling input is $(F_s/2)/4$ or 1MHz. After this we modified our single channel test-bench into a schematic and symbol cell and built up each of the interleaved channels methodically with their respective clock parameters until finishing the complete front-end (see figure3q6). Then we performed a transient simulation of the 16 independent, and added sub-sampling outputs (see figure 3q7 and 3q8 respectively), subsequently, inspecting the DFT at our reference frequency (figure 3q9) we notice we no longer have harmonics but rather a decreasing noise floor due to the stepped response at the output. Now if we consider the start of our low frequency noise floor before the start of appearance of harmonics in our response as our SFDR (original definition) we can measure:

$SFDR = 5.842\,dB + 25.91\,dB = 31.752\,dB$

We have also included the SFDR vs frequency over same frequency range (see figure 3q10) for reference, in this case no aliasing is present in our frequency spectrum or transient output waveform.

From our results, we can see the SFDR has improved substantially – due to the interleaved architecture of the S/H ADC front end – the reasoning for this is that by having multiple sampling switch branches, each sampling the same input signal but with a small time delay relative to the previous branch, we are basically sampling our input signal at multiple successive points of the input waveform, this is in principle equivalent to sampling the input at 4 times (in our case) the clock frequency if using a single-channel S/H circuit. The advantage here is that we can use a much slower clock than would otherwise be needed, the price we pay is the clocking scheme complexity which can grow quickly with increasing number of interleaved channels.

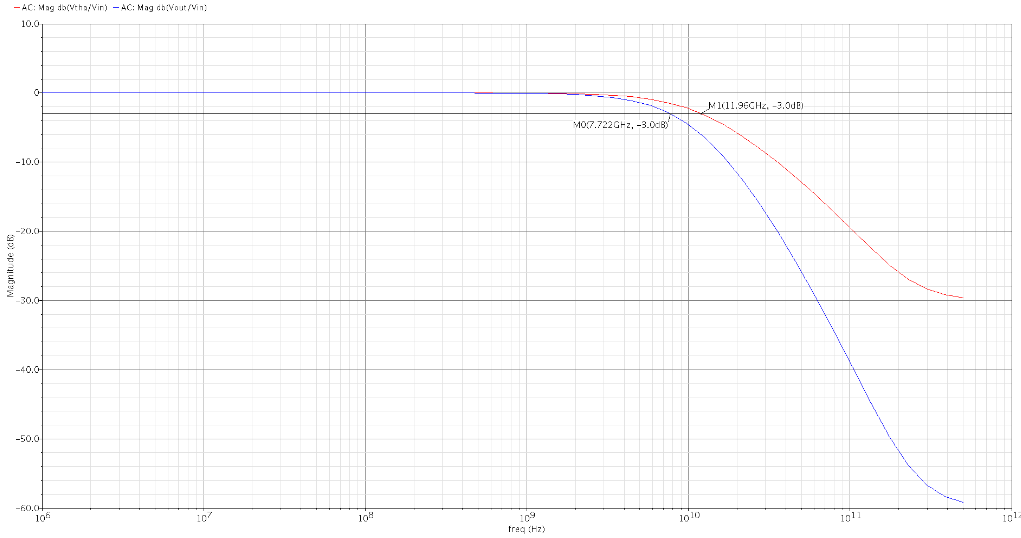

Figure 2a: 3dB AC bandwidth of the T/H and S/H circuits

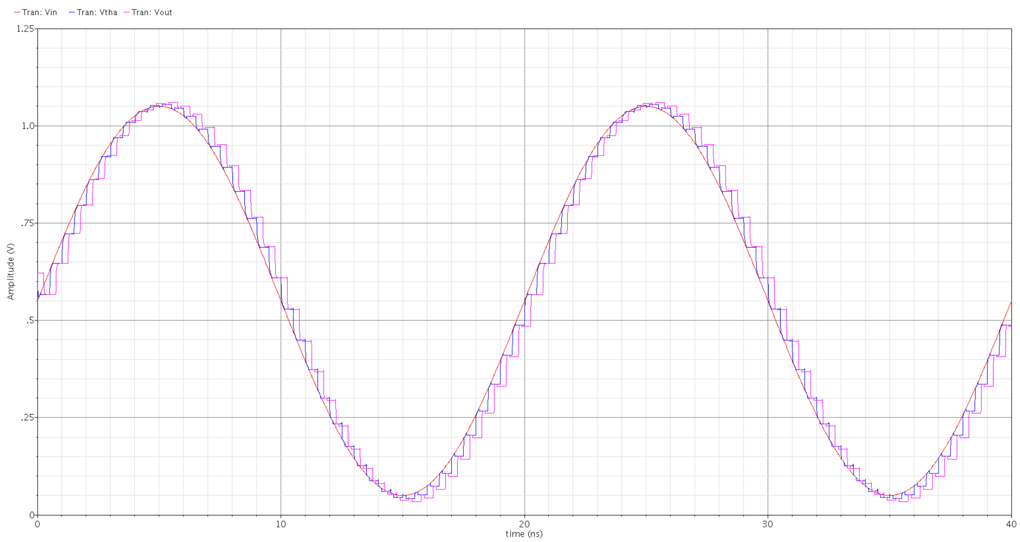

Figure 2b1: Transient response and input, T/H and S/H outputs (500mVpeak)

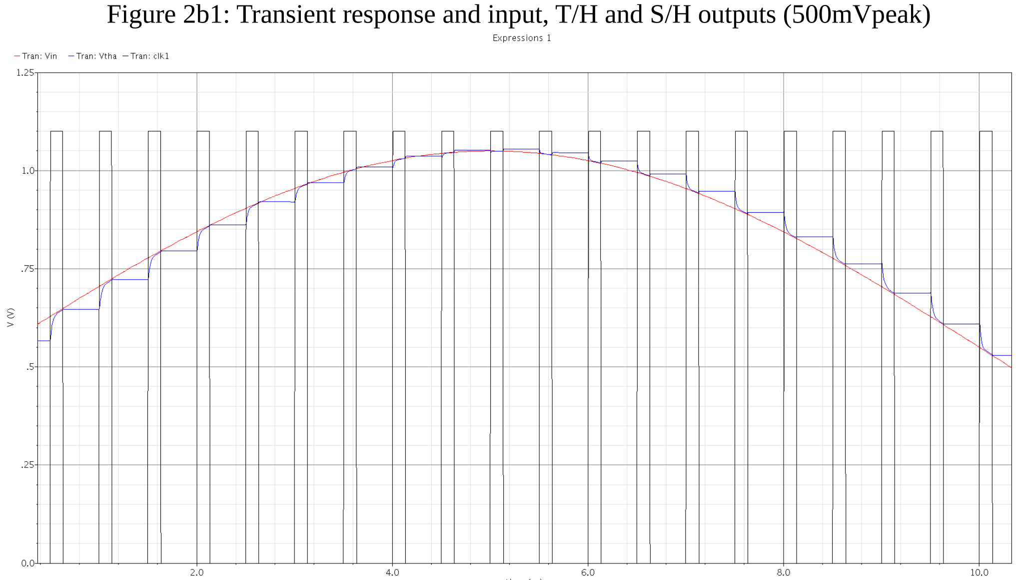

Figure 2b2: Sampling pedestal or hold step at upper swing due to charge injection

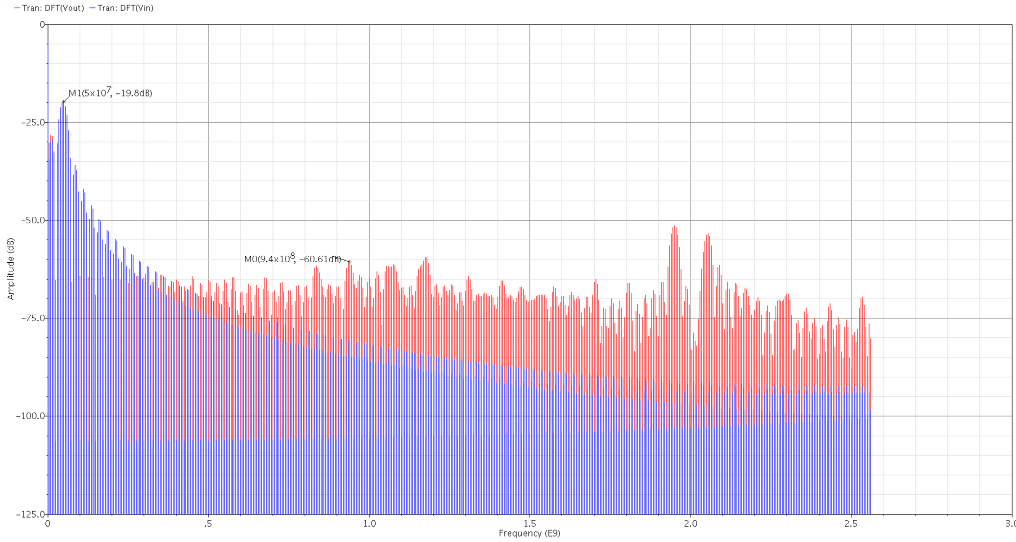

Figure 2b3: Superimposed FFT at input and output node of S/H circuit (500mVpeak)

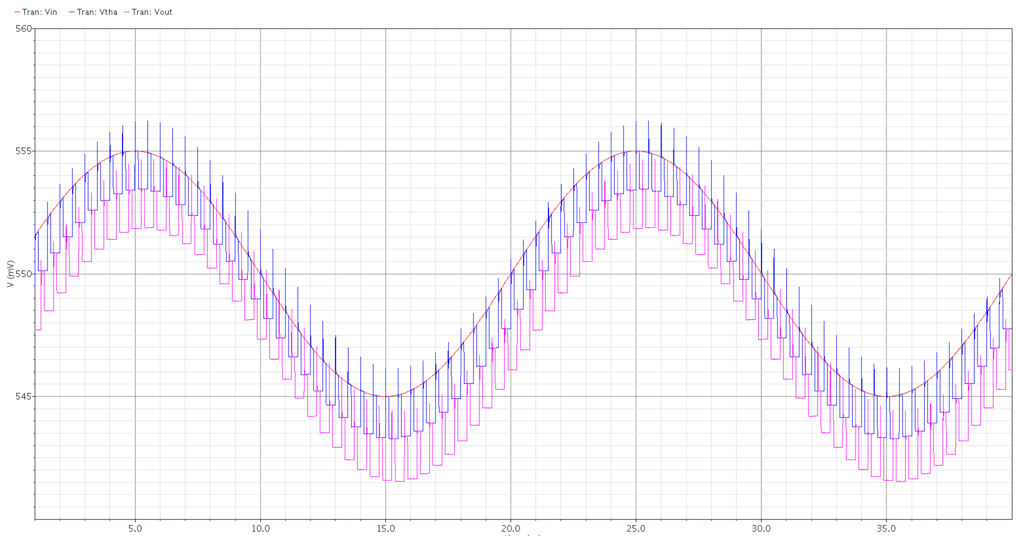

Figure 2c1: Transient response and input, T/H and S/H outputs (5mVpeak)

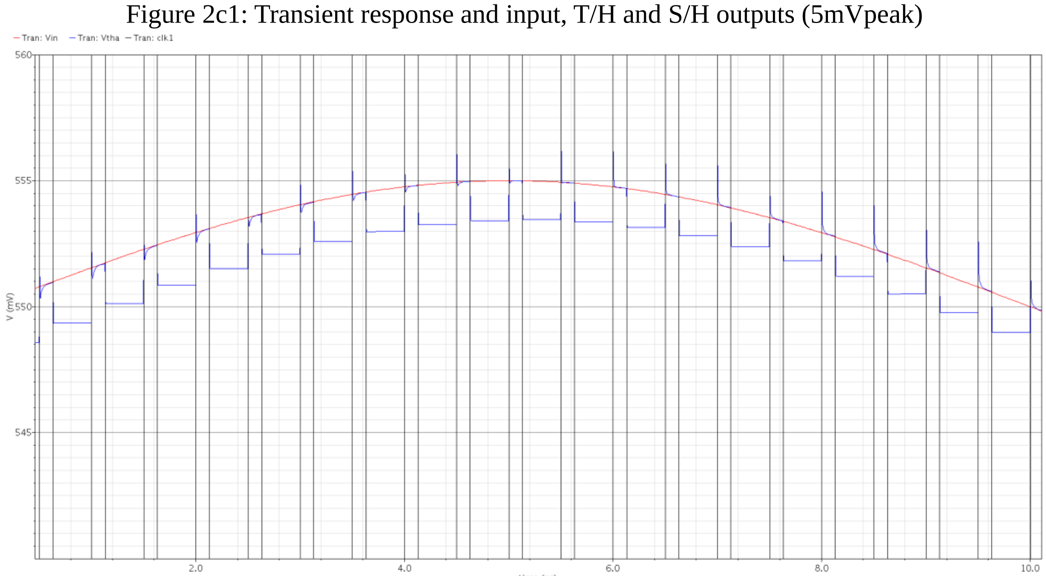

Figure 2c2: Clock feed-through and charge injection errors

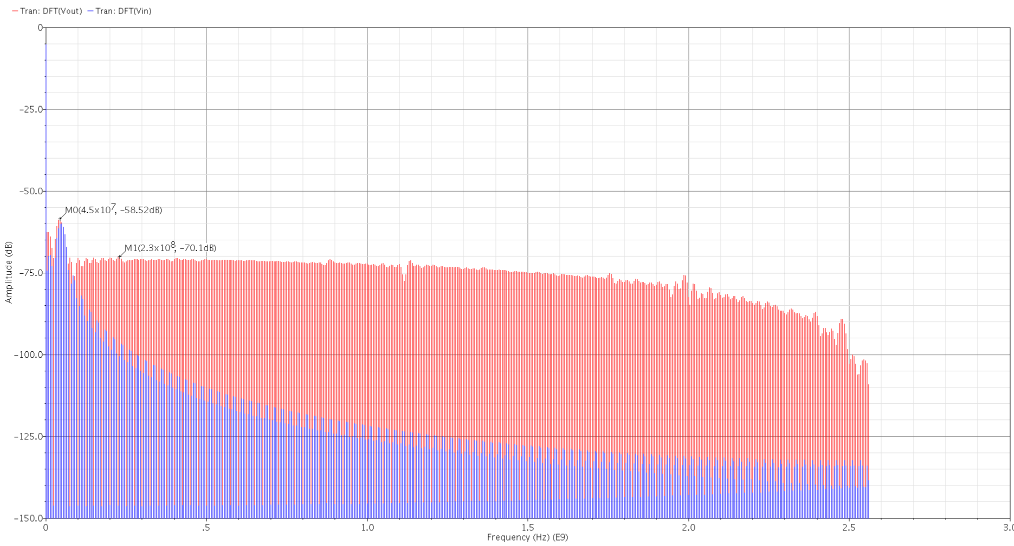

Figure 2c3: Superimposed FFT at input and output node of S/H circuit (5mVpeak)

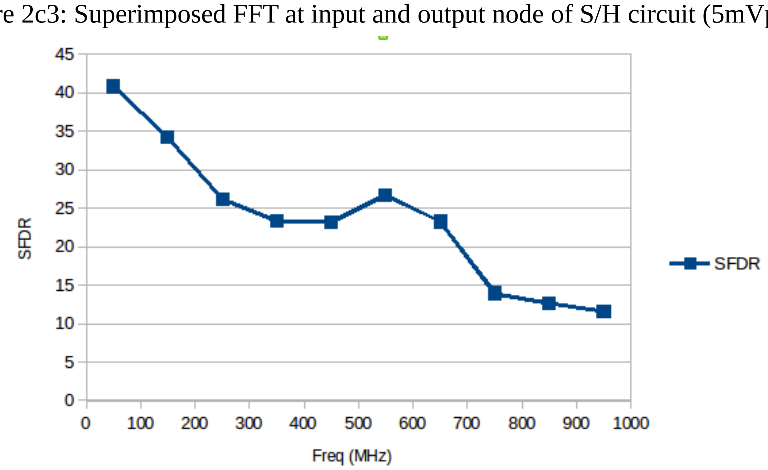

Figure 2e1: SFDR vs. Frequency for S/H circuit (500mVpeak)

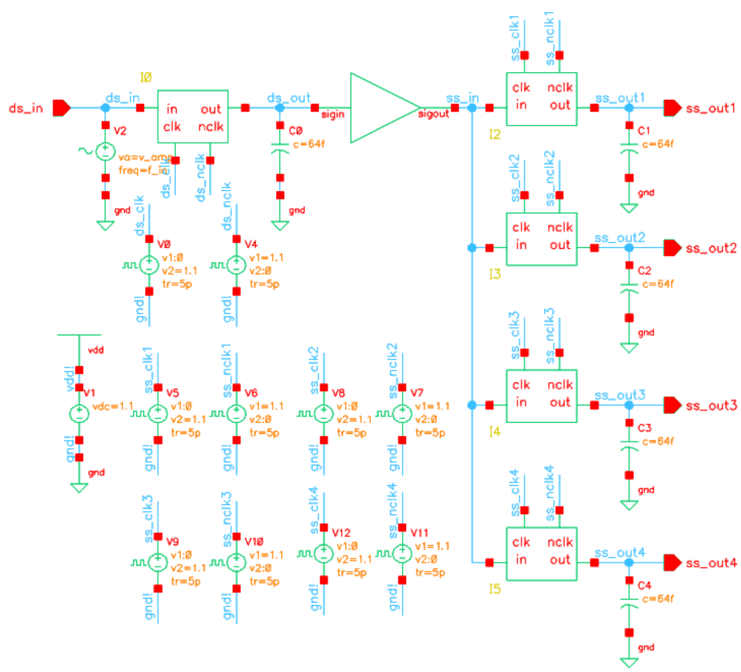

Figure 3q1: Direct-sampling one interleaved channel test-bench

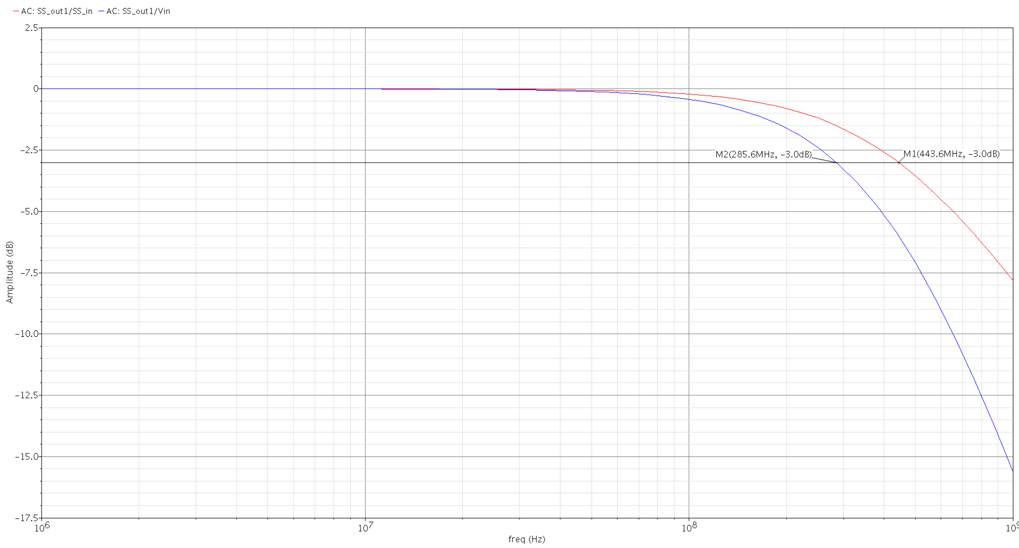

Figure 3q2a: 3dB AC bandwidth response at sampling and sub-sampling outputs (minimum dimensions)

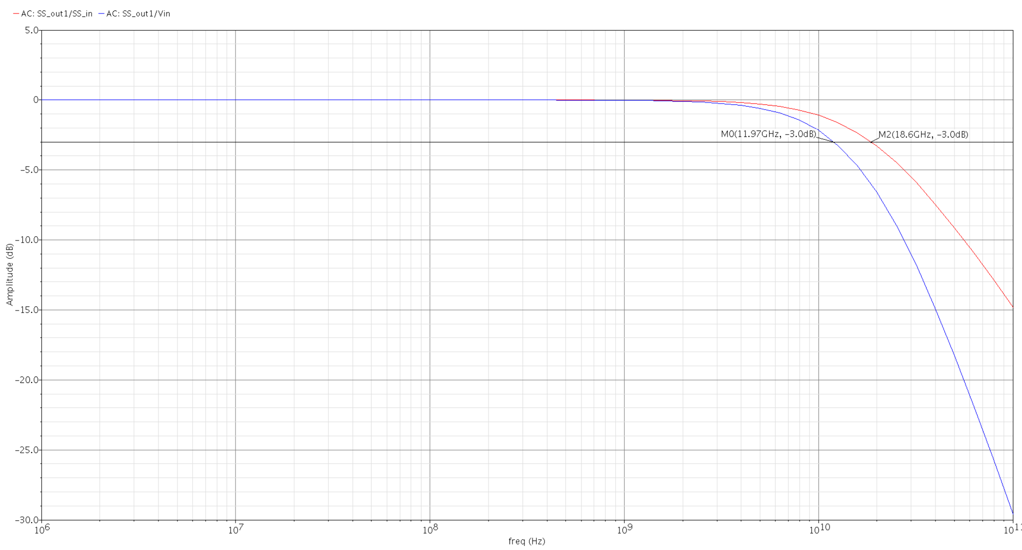

Figure 3q2b: 3dB AC bandwidth response at sampling and sub-sampling outputs (Wtotal = 10um, 10 gate fingers)

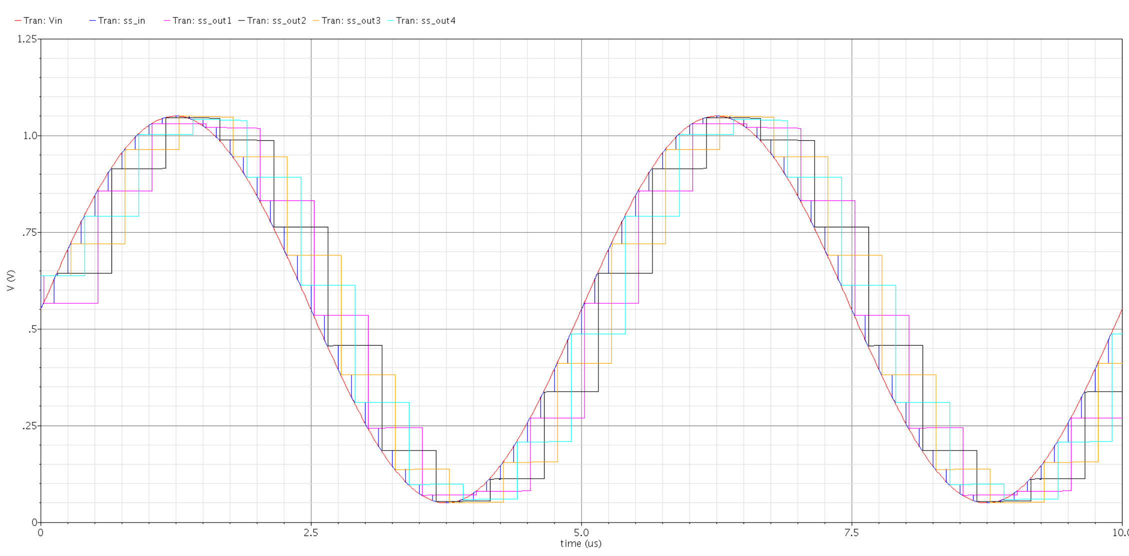

Figure 3q3: Transient response one interleaved channel (Vin, sampling and sub-sampling outputs)

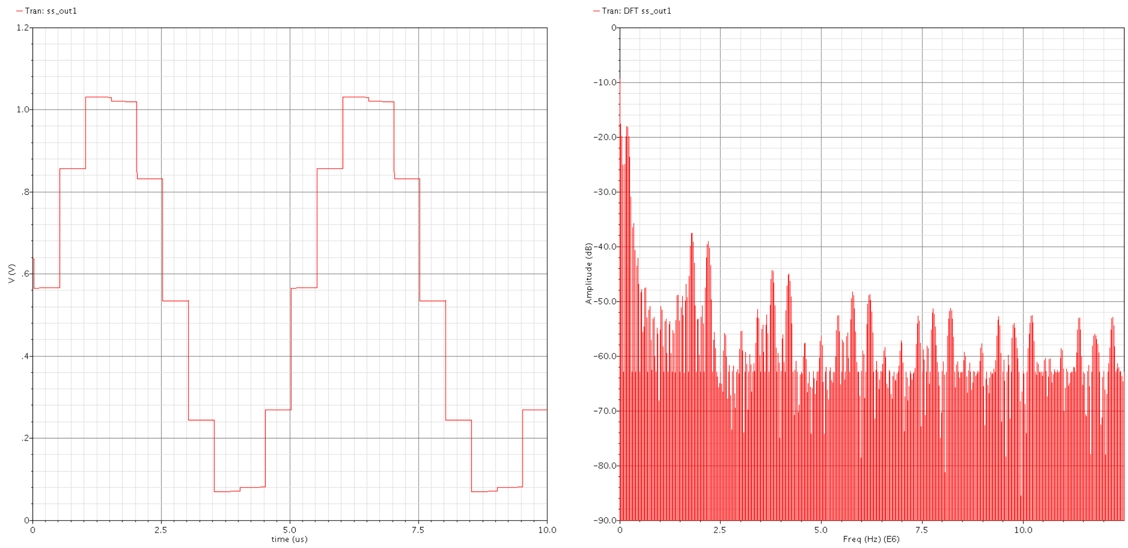

Figure 3q4: Transient response at one sub-sampling output and DFT (200KHz ref frequency)

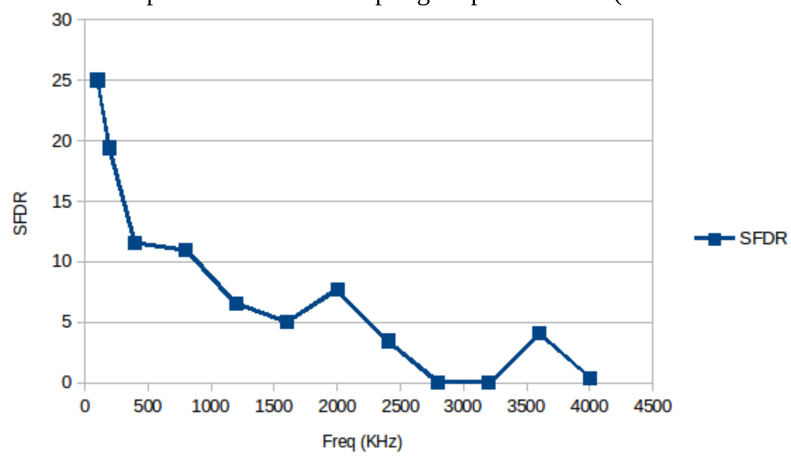

Figure 3q5: SFDR vs. Frequency at one sub-sampling output

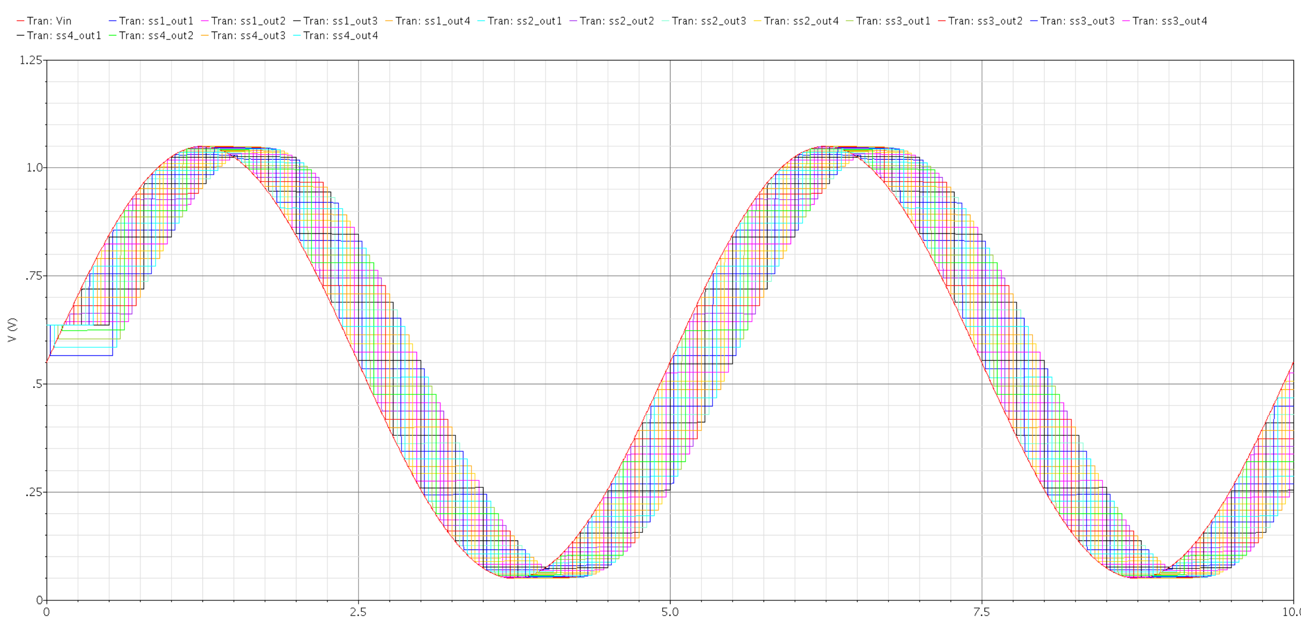

Figure 3q7: Transient simulation of the 16 independent sub-sampling outputs

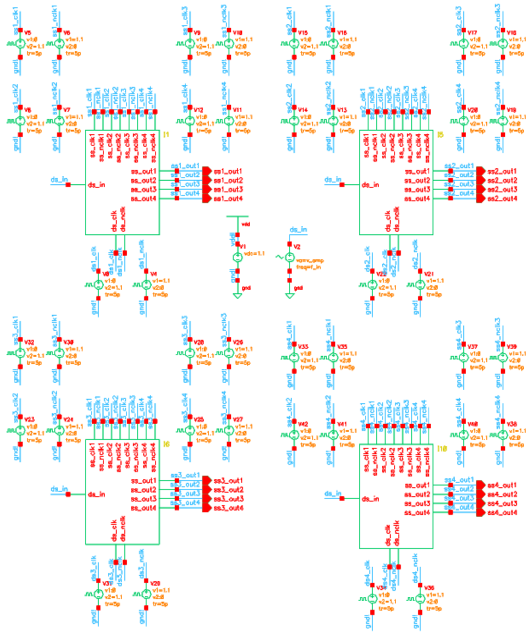

Figure 3q6a: 4x sample and hold time-interleaved ADC front end schematic

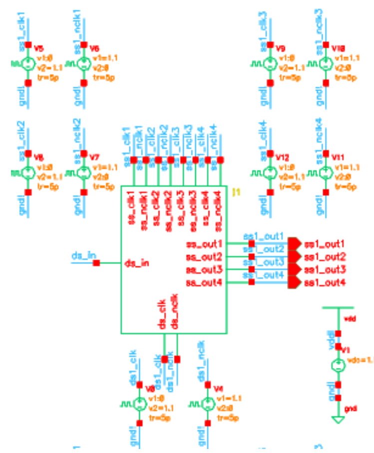

Figure 3q6b: Sample and hold time-interleaved ADC front end schematic (single channel)

Figure 3q8: Transient simulation of the 16 added sub-sampling outputs.
(note that this amplitude is not seen in practice as addition/reconstruction is performed afterwards in digital domain)

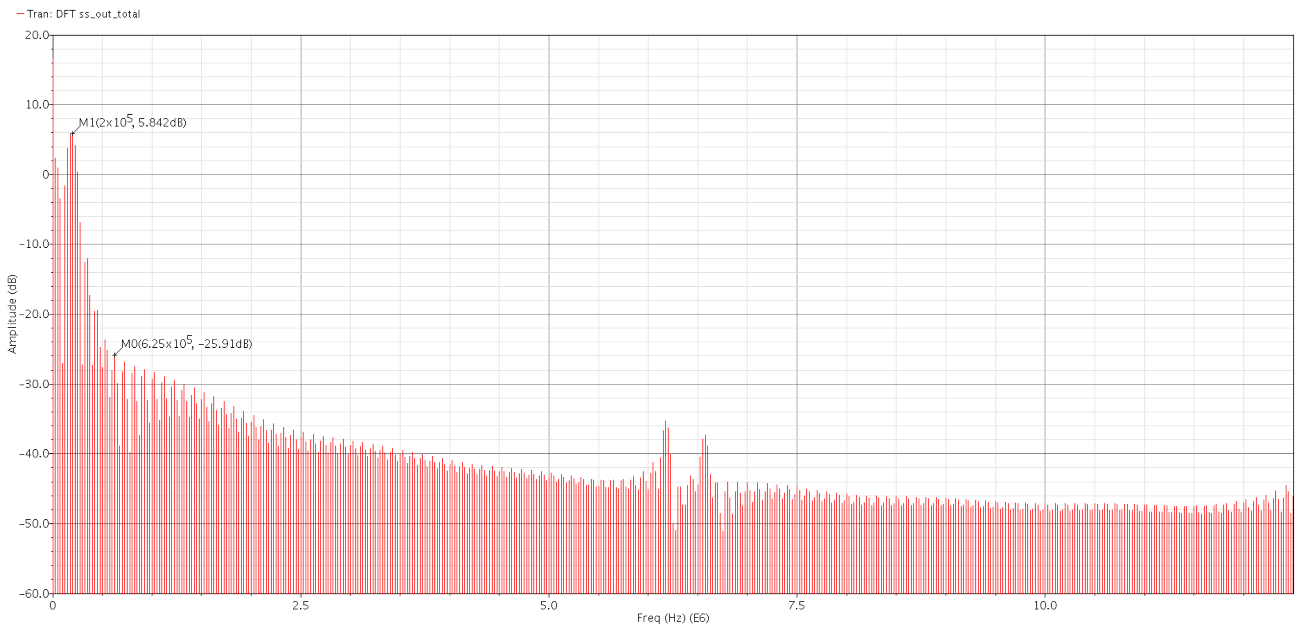

Figure 3q9: FFT of the 16 added sub-sampling outputs

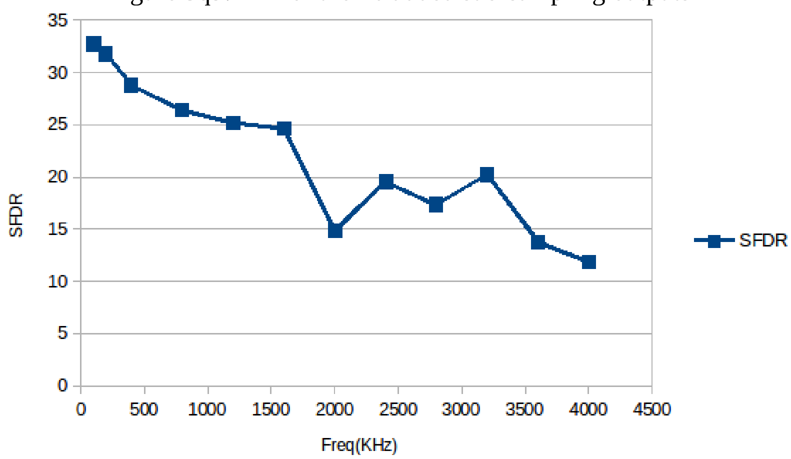

Figure 3q9: SFDR vs Frequency (at 16 added sub-sampling outputs)