Switched Capacitor Integrators and Filters

1. Preparation: As required the chapter 14 of the textbook and the course slides were reviewed and used for this assignment.

2a. MOSFET switch simulation and modelling (R=0.1Ω):
First, the circuit was biased in it's OFF condition with a low parasitic gate and substrate resistances (Vc = 0V and R = 0.1Ω). Then as an S-parameter (SP) analysis was performed and from this analysis the imaginary Y-parameters were plotted: these correspond to the imaginary admittances of our switch (see figures 2a1 and 2a2). As we can see from the imaginary admittances which increase linearly with frequency, we can extract our parasitic capacitances normalized to the device's width, mainly:

$$C'_{gs}+C'_{sb}=\frac{\Im(Y_{11}+Y_{12})}{2\pi f\, w_{total}} \qquad C'_{gd}+C'_{db}=\frac{\Im(Y_{22}+Y_{12})}{2\pi f\, w_{total}}$$

For our calculations, we extracted the value at mid-scale from our frequency sweep (5GHz), therefore we get:

$$C'_{gs}+C'_{sb}=\frac{2.204\,x10^{-4}}{2\pi 5\,x10^{9}10\,\mu}=\frac{7.01\,fF}{10\,\mu}=0.701\,fF/\mu$$

$$C'_{gd}+C'_{db}=\frac{2.282\,x10^{-4}}{2\pi 5\,x10^{9}10\,\mu}=\frac{7.26\,fF}{10\,\mu}=0.726\,fF/\mu$$

adding our parasitic capacitances per unit width together we get our OFF capacitance per unit width:

$$C'_{OFF}=C'_{gs}+C'_{sb}+C'_{gd}+C'_{db}=1.426\,fF/\mu$$

At this point we turned our switch to it's ON condition and repeated the SP analysis to obtain the real Y-parameters. Here the real admittances (simply a plotted straight line; not provided) correspond to the conductance of our switch (the inverse of the ON resistance), mainly:

$$R'_{ON}=\frac{1}{\Re(-Y_{12})\,w_{total}}=\frac{34.883\,\Omega}{10\,\mu}=\frac{3.488\,\Omega}{\mu}$$

Therefore the figure of merit for our switch at our device width (Wtotal) is:

$$FoM=R_{ON}C_{OFF}=34.95\,\Omega\,x\,14.27\,fF=497.780\,x10^{-15}\Omega\,F$$

2b. MOSFET switch simulation and modelling (R=10KΩ):

Next, the gate and substrate parasitic resistances were changed to 10KΩ. The addition of this increased parasitic resistances together with the parasitic capacitances accounts for a pole which is now brought down to (assuming single overlap capacitance ~7fF):

$$f_{pole}=1/(2\pi R_{par}C_{par})=1/(2\pi\,x\,10K\,\Omega\,x\,7\,fF)=2.276\,GHz$$

We can see this from our Y-parameter plots (figures 2b1 and 2b2). The addition of this pole at a lower frequency makes our curve non-linear and results in our calculation of parasitic capacitances becoming non-trivial. Instead we reduced the frequency range for our SP analysis from 1MHz to 100MHz, and plotted again our imaginary admittance Y-parameters (figures almost identical to 2a1 and 2a1 but over a lower frequency range). From this linear imaginary admittance curves it was then trivial to obtain our capacitances (as before):

$$C'_{gs}+C'_{sb}=\frac{2.203\,x10^{-6}}{2\pi 50\,x10^{6}10\,\mu}=\frac{7.012\,fF}{10\,\mu}=0.701\,fF/\mu$$

$$C'_{gd}+C'_{db}=\frac{2.281\,x10^{-6}}{2\pi 50\,x10^{6}10\,\mu}=\frac{7.260\,fF}{10\,\mu}=0.726\,fF/\mu$$

$$C'_{OFF}=1.427\,fF/\mu$$

We have similar values for our parasitic capacitances as should be expected (we haven't modified our intrinsic device properties).

And our ON resistance and FoM were obtained as before:

$$R'_{ON}=\frac{3.495\,\Omega}{\mu} \qquad FoM=R_{ON}C_{OFF}=498.736\,x10^{-15}\Omega\,F$$

While the FoM appears similar, it is only because we have reduced the frequency range of operation of our switch. In fact, the increase in parasitic resistances degraded the bandwidth performance of our switch substantially (below 2GHz).

3. Switched Capacitor simulation and charge injection:

The switched capacitor test-bench was put together as indicated, with the non overlapping clocks at Fs = 2GHz, subsequently a 500mVpeak sinusoid at 50MHz was applied and the transient results at input, store and output nodes were plotted vs time (see figure 3q1).

The charge injection error for a MOSFET switch is due to both the stored channel charge as well as the overlap and fringe parasitic capacitances. Specifically charge stored in the channel during the ON state must be deposited back to our sampling capacitor when the switch transitions to it's OFF state (i.e. charge injection), additionally the clock rising and falling edges represent high frequency components which are coupled to our signal through the parasitic capacitances (clock feed-through); we see both of these effects as voltage errors. The maximum error at our store node is:

$$\Delta V=309.291\,mV-305.399\,mV=3.892\,mV$$

In order to measure the SFDR at the output of our circuit, a DFT of input and output (over-imposed) was taken over 200nS with 1024 points and a rectangular window (see figure 3q3).

Measuring the dB difference between the fundamental and the maximum harmonic below Fs/2 (where our spectrum repeats) we obtain: $SFDR=-25.131\,dB-(-59.851\,dB)=34.72\,dB$

Subsequently we are asked to increase the width of our devices to assess the effect on our circuit. As the width of our switch is increased both the channel capacitance and the overlap and fringing capacitances increase leading to larger charge injection and clock feed-through errors. The maximum error at our store node is: $\Delta V=24.502\,mV$

Finally we leave purely NMOS switches resized to their original dimensions. This switch is severely limited for large swings: i.e. as the signal rises towards the positive supply, the voltage at its "source" increases and thus Vgs decreases, at some point Vgs < Vth and the transistor starts to turn OFF, at this point it can no longer conduct and track the input voltage thus limiting the voltage range of operation for this switch significantly (see figure 3q5 for reference). The maximum voltage error and the SFDR at the output of our circuit (which degraded significantly for the reasons above) are:

$$\Delta V=16.342\,mV \qquad SFDR=13.897\,dB$$

4. Discrete-time bandpass filter design:

a. Hand design equations, Z-transfer function, component values and schematic

we were asked to design a discrete-time switched-capacitor band-pass filter with the following requirements: $F_o=160\,MHz$ or $T_o=6.25\,nS$ $Q=6$ $Gain=H_o=6\,V/V$ $V_{supply}=1.1\,V/V$

First we chose our sampling frequency to be 10x our center frequency i.e. $F_o = F_s/10$ where $F_s = 1.6\,GHz$

Now, normalizing our center frequency to our sampling frequency, we get (in discrete-time domain):

$$w_{o,dt} = 2\pi f_o/f_s = 2\pi/10 = 0.2\pi\, rad/sample$$

Then, converting to continuous time (normalized to the sampling clock): we call this continuous time normalized domain "p", it is mostly used for convenience in our calculations. (as we are familiar with them in continuous time), therefore:

$$\Omega_o = \tan(0.2\pi/2) = 324.920\,x\,10^{-3}\, rad/second$$

Plugging in into our standard continuous time band pass equation:

$$H(p) = \frac{k_1 p}{p^2 + (\Omega_o/Q)\,p + \Omega_o^2} \quad \text{where} \quad k_1 = H_o \frac{\Omega_o}{Q} \quad ,$$

where H_o is our pass band gain.

Therefore, $k_1 = \dfrac{0.9\,x\,324.920\,x\,10^{-3}}{6} = 48.738\,x\,10^{-3}$

And our equation in the continuous time "p" domain becomes:

$$H(p) = \frac{48.738\,x\,10^{-3}\,p}{p^2 + 54.153\,x\,10^{-3}\,p + 105.573\,x\,10^{-3}}$$

Now, we need to transform back our transfer function to the discrete-time Z domain using the bi-linear transform i.e:

We are keeping the original variables while we work the algebra.

$$H(z) = \frac{k_1 \frac{z-1}{z+1}}{(\frac{z-1}{z+1})^2 + (\Omega_o/Q)\frac{z-1}{z+1} + \Omega_o^2}$$

Then multiplying top and bottom by $(Z+1)^2$

$$H(z) = \frac{k_1 (z-1)(z+1)}{(z-1)^2 + (\Omega_o/Q)(z-1)(z+1) + \Omega_o^2 (z+1)^2}$$

Expanding we get:

$$H(z) = \frac{k_1 (z-1)(z+1)}{(z-1)^2 + (\Omega_o/Q)(z-1)(z+1) + \Omega_o^2 (z+1)^2}$$

$$H(z) = \frac{k_1 (z^2-1)}{z^2 - 2z + 1 + z^2\Omega_o/Q - \Omega_o/Q + \Omega_o^2 z^2 + 2\Omega_o^2 z + \Omega_o^2}$$

Collecting/factoring terms in the denominator we get:

$$H(z) = \frac{k_1 z^2 - k_1}{z^2(1 + \Omega_o/Q + \Omega_o^2) + z(-2 + 2\Omega^2) + 1 - \Omega/Q + \Omega^2}$$

Substituting for our known values we get:

$$H(z) = \frac{48.738\,x\,10^{-3} z^2 - 48.738\,x\,10^{-3}}{1.160\,z^2 - 1.789\,z + 1.051}$$

Finally dividing everything by 1.160 to conform to our canonical equation form, we get our transfer function in the DT Z domain (note the negative sign for the inverting band-pass response)

$$H(z) = -\frac{42.015\,x\,10^{-3} z^2 - 42.015\,x\,10^{-3}}{z^2 - 1.542\,z + 906.034\,x\,10^{-3}}$$

comparing our equation with that for a high-Q SC biquad filter:

$$H(Z) = \frac{a_2 z^2 + a_1 z + a_0}{z^2 + b_1 z + b_0}$$ therefore our coefficients are:

$a_2 = 42.015\,x\,10^{-3}$ $a_1 = 0$ $a_0 = -42.015\,x\,10^{-3}$
$b_1 = -1.542$ $b_0 = 906.034\,x\,10^{-3}$

Our coefficients agree with values computed from online DT biquad calculators[1][2].

Equating these with our design equations:

$k_4 = k_5 = \sqrt{1 + b_0 + b_1} = 603.352\,x\,10^{-3}$ $k_1 = 0$
$k_2 = (a_2 - a_0)/k_5 = 139.272\,x\,10^{-3}$ $k_3 = 42.015\,x\,10^{-3}$
$k_6 = (1 - b_o)/k_5 = 155.74\,x\,10^{-3}$

Therefore, our component values (using a reference capacitances $C_1 = C_2 = 100\,pF$):

$k_1 C_1 = 0$ (open branch) $k_2 C_1 = 13.927\,pF$
$k_3 C_2 = 4.201\,pF$ $k_4 C_1 = 60.335\,pF$ $k_4 C_1 = 60.335\,pF$
$k_6 C_1 = 15.574\,pF$

The maximum capacitance spread is: 14.362

For simulating our circuit our non overlapping clocks had the following properties (Fs: 1.6GHz, pulse width: 25% of period or 156.25pS, Trise and Tfall: 10% of pulse width or 15.625pS, delay for phase2: 312.5pS) (See figure 4a1 for the schematic and 4a2 for CMOS switch cell)

b. Transient waveforms at input and output (Vin = 500mV)

Initially the circuit bias point experienced large drift towards the supply rails, this was finally discovered to be due to the use of large switches with similar dimensions from previous questions (which contributed charge injection and clock feed-through errors which get integrated over time). Re-sizing the switches to the minimum geometry decreased the parasitic capacitances and reduced the error which solved our drift issue. (See figure 4b for the transient simulation)

c. Two-tone inter-modulation distortion

First, two input signals with amplitude of 500mV at F1 = 150MHz and F2 = 170MHz were applied as inputs to the circuit (See figure 4c1 for the inter-modulated input), then a DFT at the output was computed (See figure 4c2 for the DFT of the output), finally the OIP3 was computed (we only look at one sideband):

$$OIP_3 = I_{d1} - ID_3/2 = -44.76\,dB - (-63.01\,dB + 44.76\,dB)/2$$

$$OIP_3 = -35.635\,dB$$

and since we know the gain of the circuit and OIP3 level, we can calculate the IIP3. We know the equivalent gain from output to input is 1/0.9 or ~1.1V or 0.915dB therefore:

$$IIP_3 = -35.635\,dB + 0.915\,dB = -34.720\,dB$$

Now repeating the process at 100mV amplitude:

$$OIP_3 = I_{d1} - ID_3/2 = -24.4\,dB - (-42.45\,dB + 24.4\,dB)/2$$

$$OIP_3 = -15.375\,dB$$

$$IIP_3 = -15.375\,dB + 0.915\,dB = -14.46\,dB$$

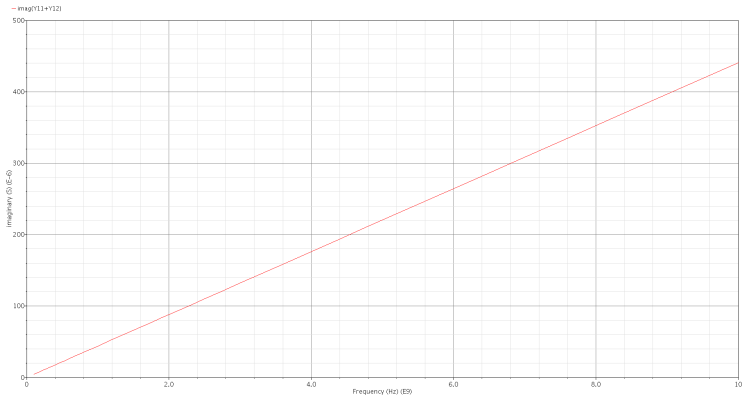

Figure 2a1: Imaginary admittances Y11 and Y12

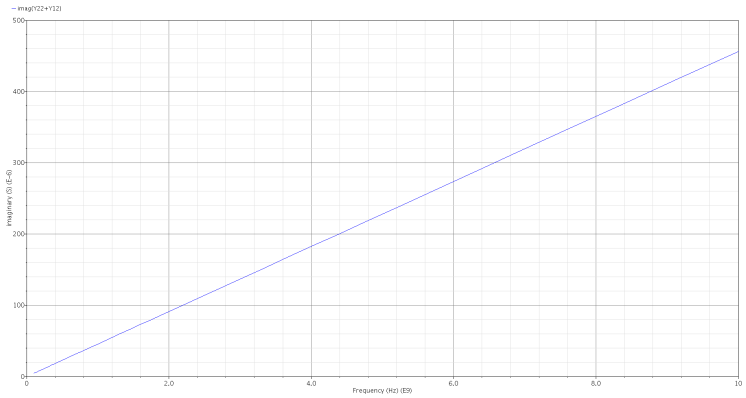

Figure 2a2: Imaginary admittances Y22 and Y12

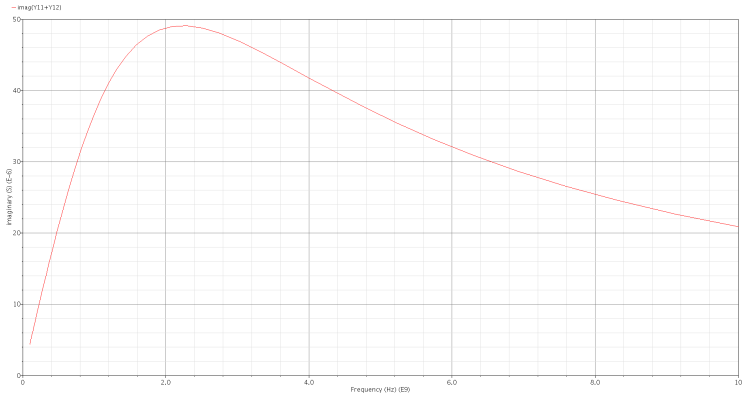

Figure 2b1: Imaginary admittances Y11 and Y12 (increased parasitic resistance)

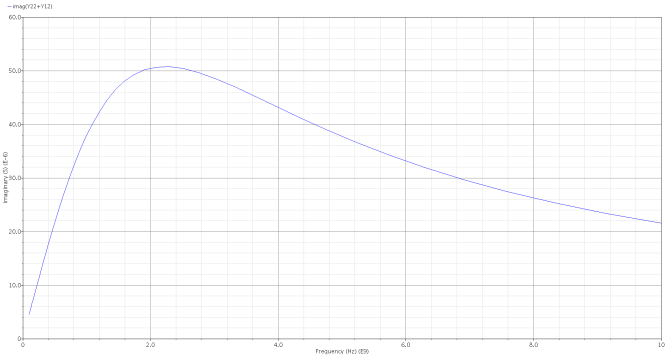

Figure 2b2: Imaginary admittances Y22 and Y21 (increased parasitic resistance)

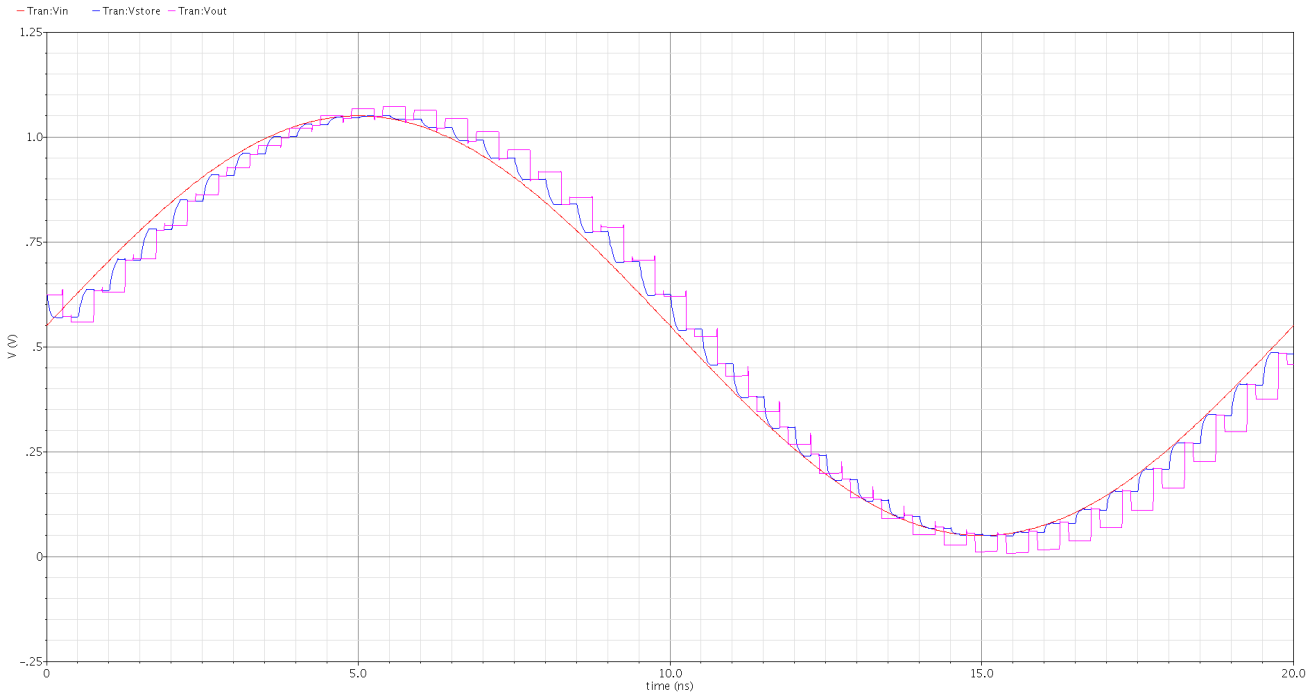

Figure 3q1: Transient simulation at input, store and output nodes

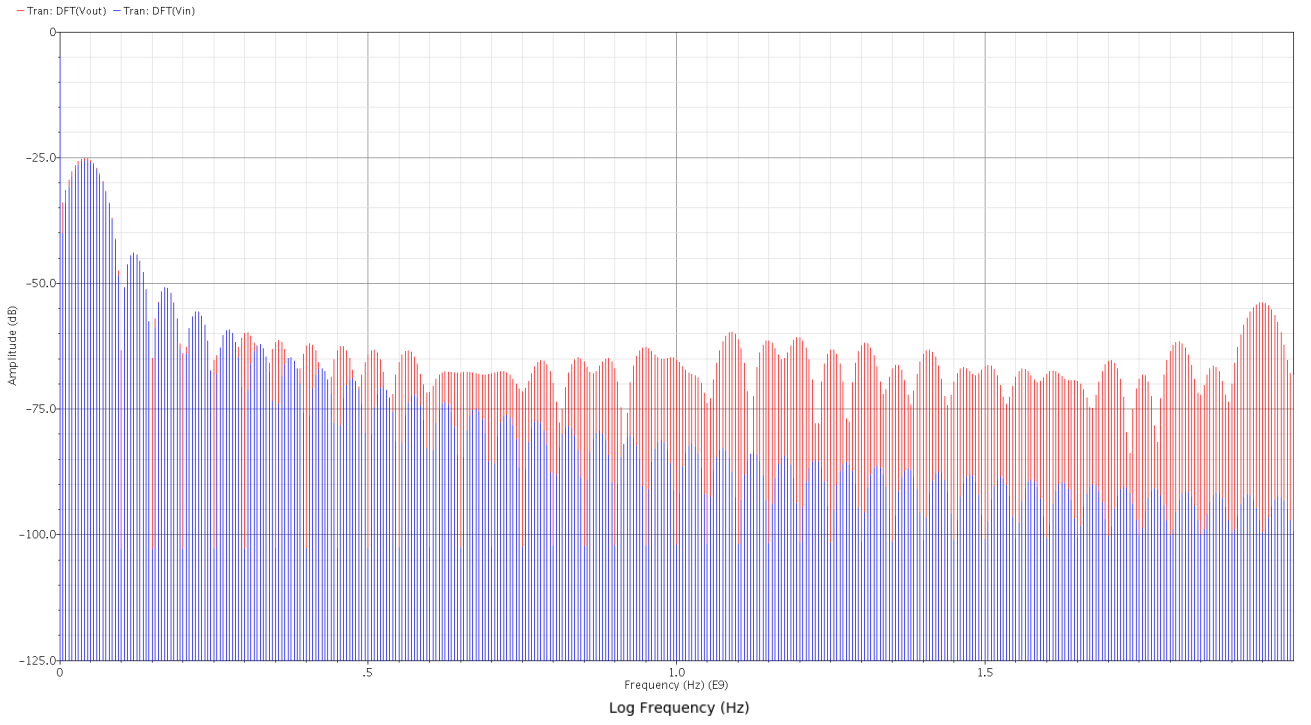

Figure 3q3: DFT of input and output (over-imposed) *note typo, this is linear frequency not logarithmic

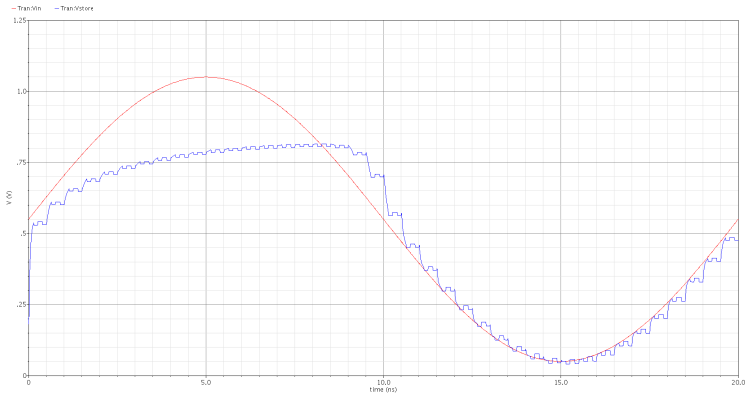

Figure 3q5: Transient simulation NMOS switch store node (limited range)

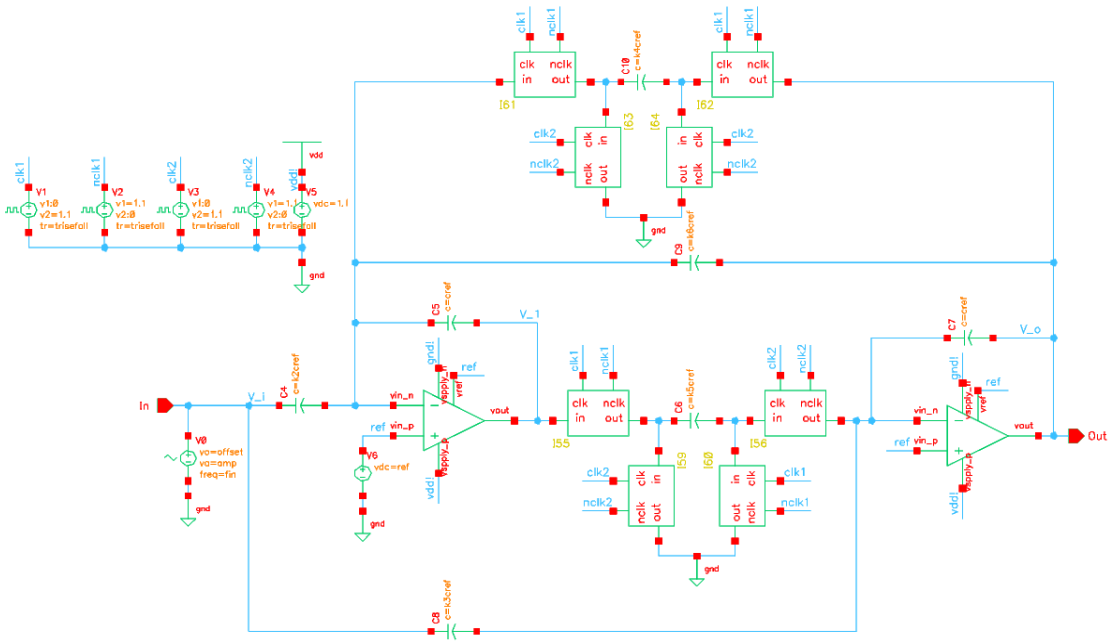

Figure 4a1: Schematic diagram High-Q DT SC Band-pass filter

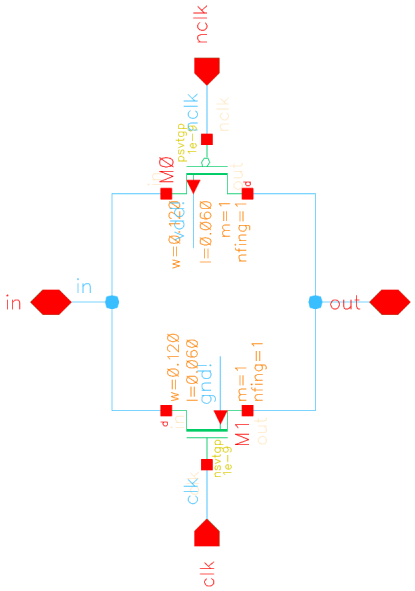

Figure 4a2: Schematic diagram of CMOS switch (transmission gate) with dimensions

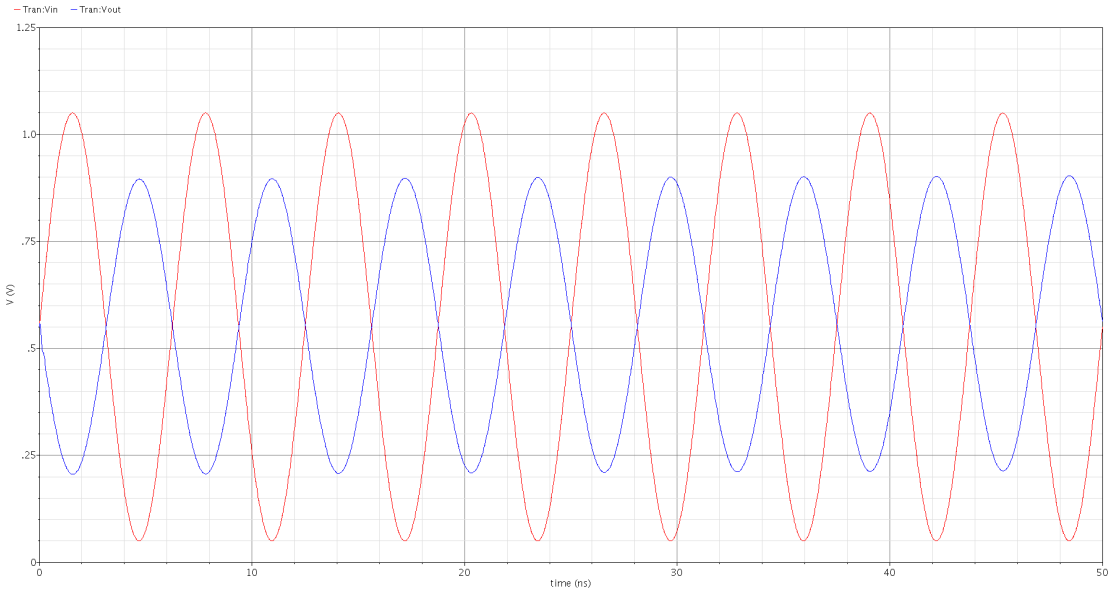

Figure 4b: Transient simulation at input and output of circuit (Vin = 500mVpeak)

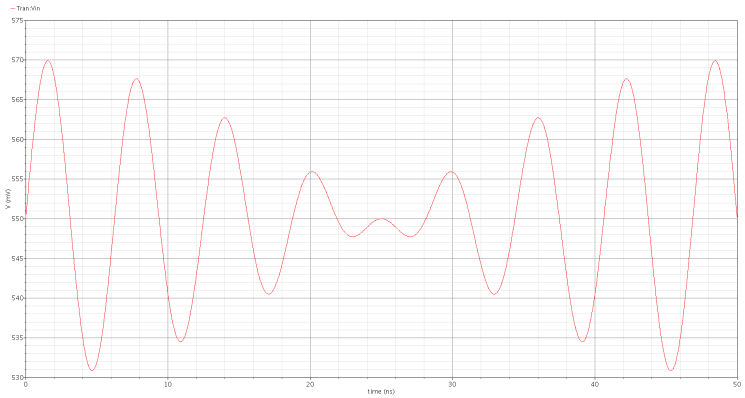

Figure 4c1: Two 10mV tones at 150MHz and 170MHz added at input

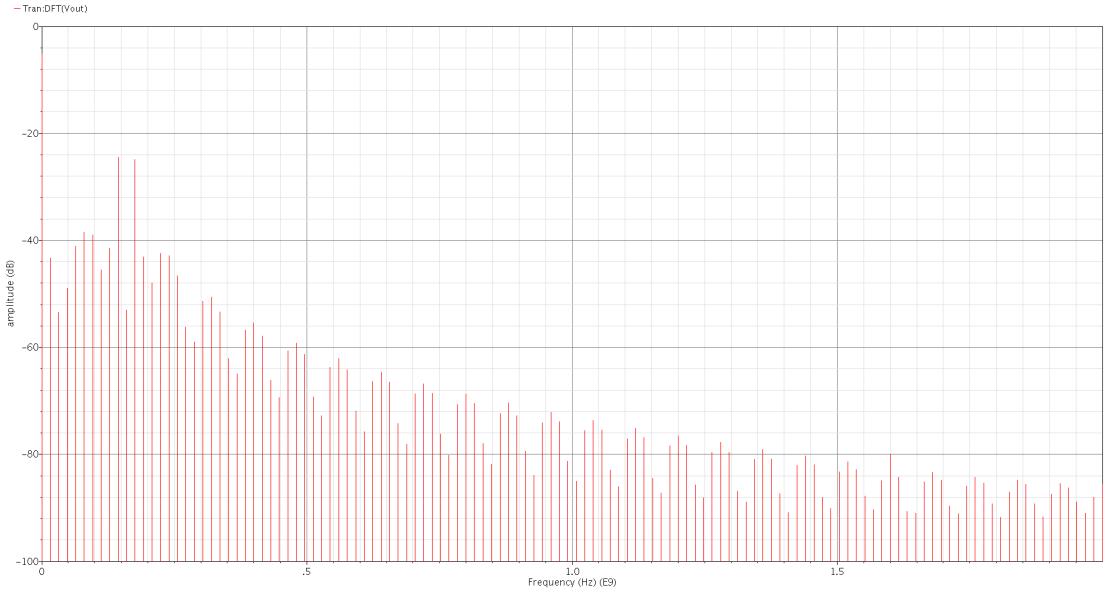

Figure 4c2: DFT of output, inter-modulation two tone test (10mV)

References [1][2]: http://www.earlevel.com/main/2013/10/13/biquad-calculator-v2, https://arachnoid.com/BiQuadDesigner