Design of a low-noise phase locked loop

1. Preparation: The course slides, PLL application note and the chapters 9 and 19 in the book were reviewed. All modeling for this assignment was done using Python packages Numpy, Scipy and matplotlib (pyplot module).

2. Reference oscillator phase noise model: The general phase noise model for an oscillator is as follows (using book notation for normalized one-sided phase noise power spectral density):

$$S_{\phi,ref}(\Delta f)=\frac{en_3}{f^3}+\frac{en_2}{f^2}+\frac{en_1}{f}+\frac{KTF}{P_{avs}} \quad \text{in} \quad rad^2/Hz$$

For this specific reference oscillator we are told: at large offset frequencies we have a noise floor of $-160\,dBc/Hz$ and a $1/f^2$ profile everywhere else with $-140\,dBc/Hz$ at a $10\,KHz$ offset, therefore the phase noise model for this reference oscillator consist of only the following terms:

$$S_{\phi,ref}(\Delta f)=\frac{en_2}{f^2}+\frac{KTF}{P_{avs}}$$

Here KTF/P_{avs} is the constant noise floor of the oscillator and is dominant at higher frequencies, and the $1/f^2$ term is due to white noise sources and is dominant at lower frequencies where it is added to our noise floor. Therefore converting from dBc/Hz we get:

$$S_{\phi,ref}(\Delta f\to\infty)=KTF/P_{AVS}=10^{(-160/10)}=10^{-16}$$

$$S_{\phi,ref}(\Delta f=10\,KHz)=en_2/f^2+KTF/P_{avs}=10^{(-140/10)}=10^{-14}$$

$$\therefore \quad en_2=(10^{-14}-10^{-16})\,x\,(10\,KHz)^2=9.9\,x\,10^{-7}$$

Therefore, all the terms for our reference phase noise model*:*

$$en_1=0 \qquad en_2=9.9\,x\,10^{-7}\,rad^2\,Hz \qquad en_3=0$$
$$KTF/P_{avs}=10^{-16}\,rad^2/Hz$$

And the complete phase noise equation for our reference is*:*

$$S_{\phi,ref}(\Delta f)=\frac{9.9\,x\,10^{-7}}{f^2}+10^{-16}\,rad^2/Hz$$

The plot of the phase noise for our reference in dBc/Hz vs logarithmic frequency, was modeled using Python. *(*see figure 2*)*

Here we can see a noise floor of -160dBc/Hz at large frequencies, a phase noise of -140dBc/Hz at a 10KHz offset and a slope of -20dBc/decade at low frequencies as expected.

3. Voltage-controlled oscillator phase noise model:

For our VCO we are told: at large offset frequencies we have a noise floor of $-140\,dBc/Hz$ and a $1/f^3$ profile everywhere else with $-100\,dBc/Hz$ at a $1\,MHz$ offset, therefore the phase noise model for this cross-coupled VCO consists of only the following terms: $S_{\phi,vco}(\Delta f)=\frac{en_3}{f^3}+\frac{KTF}{P_{avs}}$

Here the $1/f^3$ term is due to 1/f or flicker noise sources common in CMOS devices and is added to our noise floor at low frequencies. Converting from dBc/Hz we get:

$$S_{\phi,vco}(\Delta f\to\infty)=KTF/P_{AVS}=10^{(-140/10)}=10^{-14}$$

$$S_{\phi,vco}(\Delta f=1\,MHz)=en_3/f^3+KTF/P_{avs}=10^{(-100/10)}=10^{-10}$$

Therefore, all the terms for our VCO phase noise model*:*

$$en_1=0 \qquad en_2=0 \qquad en_3=9.999\,x\,10^7$$
$$KTF/P_{avs}=10^{-14}\,rad^2/Hz$$

And the complete phase noise equation for our VCO is:

$$S_{\phi,vco}(\Delta f)=\frac{9.999\,x\,10^7}{f^3}+10^{-14}\,rad^2/Hz$$

For the plot of the phase noise for our VCO in dBc/Hz vs logarithmic frequency (see figure 3) we can see a noise floor of -140dBc/Hz at large frequencies, a phase noise of -100dBc/Hz at a 1MHz offset and a slope of -30dBc/decade at low frequencies as expected.

4. Third-order PLL Design:

Given the previous reference and VCO specifications plus the additional requirements provided for our PLL:

$$f_{osc}=56-58\,GHz \qquad K_{vco}=2200\,MHz/V \qquad Lock\,time<5\,\mu S$$
$$f_{ref}=224\,MHz \qquad V_{supply}\le 1.1\,V$$

a. PLL design components and parameters: In order to design our PLL, we followed a similar procedure to that outlined on Lecture 12 slides 21 and 22 (also on page 753 in the textbook):

(1) Given $f_{ref}=224\,MHz$ we chose $f_{osc}=56\,GHz$ in order to have an integer division ratio $N=250$

(2) $Q=0.5$ was chosen to allow for both a quick phase lock as well as realistic IC components.

(3) We chose the loop bandwidth to be one tenth of the reference frequency to ensure loop stability i.e. $f_{3db}=22.4\,MHz$ or $w_{3db}=140.743\,x\,10^6\,rad/sec$

(4) We chose $w_{pll}=0.4\,w_{3db}=56.297\,x\,10^6\,rad/sec$ for Q = 0.5 as recommended.

(5) Given our equation for $C_1=I_{ch}\,x\,K_{vco}/(2\pi\,N\,w_{pll}^2)$ we chose a charge pump current that would yield realizable IC values for C1 and later C2: $I_{ch}=2\,mA$ and $C_1=5.554\,pF$

(6) Our zero is located at $w_z=Qxw_{pll}=28.149\,x\,10^6\,rad/sec$, and the resistor for our loop filter: $R=1/(w_z\,x\,C_1)=6.396\,k\Omega$

(7) The loop filter glitch suppression capacitor was chosen to be one tenth of C1 $C_2=C_1/10=0.555\,pF$ as recommended for Q = 0.5

Hence, we have the design components/parameters for our PLL:

$$N=250 \qquad I_{ch}=2\,mA \qquad R=6.396\,k\Omega \qquad C_1=5.554\,pF$$
$$C_2=0.555\,pF$$

b. PLL open loop response: From our standard 2nd order PLL equation (19.33 in the textbook) and given an additional pole, the open loop response of a 3rd order PLL with $C_1\gg C_2$:

$$L(s)=\frac{w_{pll}^2(1+s/w_z)}{s^2(1+s/w_{p3})} \quad \text{where}$$

$$w_{pll}=56.297\,x\,10^6\,rad/sec \qquad w_z=28.149\,x\,10^6\,rad/sec$$

and $w_{p3}=w_z(\frac{C_1+C_2}{C2})=309.842\,x\,10^6\,rad/sec$

The expression for the open loop gain of our PLL (magnitude and phase) was evaluated and plotted vs angular frequency from $10^6\,rad/s$ to $10^{10}\,rad/s$ (see figure 4b)

c. 3dB bandwidth, unity gain frequency and phase margin: From the magnitude response plot (figure 4b top) we can

recognize the following important frequencies (vertical markers from left to right): we start with a -40db/decade slope due to two poles at the origin until we reach our zero (1st marker), then we continue with a slope of -20db/decade passing through our PLL frequency (2nd marker), transition frequency (3rd marker) and loop bandwidth frequency (4th marker), finally we reach our 3rd pole frequency where the slope decreases again to -40 dB/decade (5th marker).

We can calculate our unity gain transition frequency:

$$w_t = \frac{w_{pll}}{\sqrt{2}}\sqrt{\frac{1}{Q^2}+\sqrt{\frac{1}{Q}+4}} = 101.096\,x10^6\,rad/sec$$

And from before, the additional angular frequencies marked in the open loop response are as follows (for reference):

$$w_z = 28.149\,x10^6\,rad/sec \qquad w_{pll} = 56.297\,x10^6\,rad/sec$$

$$w_{3db} = 140.743\,x10^6\,rad/sec \qquad w_{p3} = 309.842\,x10^6\,rad/sec$$

From our open loop phase response plot (figure 4b bottom), the vertical length of our marker at w_t identifies the phase margin.

For our case: $phase\,margin = 180° - 123.606° = 56.394°$
Therefore, it achieves a faster lock than were we to have 2nd-order PLL, at the cost of less stability.

d. PLL output phase noise: To calculate the output phase noise of the PLL, we first have to calculate the phase noise due to each of the major contributor blocks: i.e. take the intrinsic (input-referred) phase noise of each block and pass it through its respective phase transfer function, mainly:

Phase noise of reference oscillator as input to PLL

$$S_{\phi,ref}(f) = \frac{9.9\,x10^{-7}}{f^2} + 10^{-16}\,rad^2/Hz$$

Phase transfer function for overall PLL

$$H(s) = N\frac{(1+s/w_z)}{(1+s/w_z+s^2/w_{pll}^2)}$$

Therefore, the output phase noise due to our reference:

$$S_{\phi out,\text{due to ref}}(f) = S_{\phi,ref}(f)\,x\,|H(s)|^2$$

Then, phase noise of VCO

$$S_{\phi,vco}(f) = \frac{9.999\,x10^7}{f^3} + 10^{-14}\,rad^2/Hz$$

Phase transfer function for VCO

$$H_{vco}(s) = \frac{(s^2/w_{pll}^2)}{(1+s/w_z+s^2/w_{pll}^2)}$$

And the output phase noise due to our VCO:

$$S_{\phi out,\text{due to vco}}(f) = S_{\phi,vco}(f)\,x\,|H_{vco}(s)|^2$$

Finally, phase noise of our loop filter *(resistor thermal noise)*

$$S_{\phi,vco}(f) = 4\,KTR$$

Phase transfer function for loop filter

$$H_n(s) = \left(\frac{Nx2\pi}{I_{ch}\,x\,R}\right)\frac{(s/w_z)}{(1+s/w_z+s^2/w_{pll}^2)}$$

And the output phase noise due to our loop filter:

$$S_{\phi out,\text{due to lf}}(f) = S_{\phi,lf}(f)\,x\,|H_n(s)|^2$$

Finally we add all of the output phase noise components, to come up with the total output phase noise:

$$S_{\phi out}(f) = S_{\phi out,\text{due to ref}}(f) + S_{\phi out,\text{due to vco}}(f) + S_{\phi out,\text{due to lf}}(f)$$

At this point we plot the output phase noise from each major contributor block together with the total output phase noise of our PLL. (see figure 4d)
At 1 MHz (vertical marker in the figure) the main contributor to the total output phase noise of the PLL is the reference. Intuitively we can see this makes sense: the phase noise floor for the reference is -160dBc/Hz, now as the reference phase noise is applied to the phase transfer function of the PLL, it is amplified by the gain of the transfer function at low frequencies (N=250), this corresponds to an added offset in a logarithmic (dBc) scale: thus
$-160\,dBc + 10\log(250) = -112.041\,dBc$ and this agrees with the output phase noise at 1MHz from our plot.
Additionally, note that the second major contributor to our total output phase noise is the loop filter, we can reduce this figure by increasing the charge pump current, however note that this would only bring a marginal improvement as the output phase noise is bounded by the noise due to our reference oscillator which is more dominant.

e. RMS phase error and jitter

First, to calculate RMS phase error (in rads) and jitter (in seconds):
RMS phase error

$$\theta_{rms} = \sqrt{2\int_{1\,KHz}^{100\,MHz} S_{\phi out}(fm)\,dfm}$$

The representation of phase error in the time domain is RMS jitter:

$$\sigma_{jrms} = \frac{1}{2\pi f_{out}}\,x\,\theta_{rms}$$

The integrated phase noise from 1KHz to 100MHz was calculated using the Python package Scipy, module integrate – numerical QUADPACK integration. The factor of 2 in the phase phase error equation accounts for the fact that we are using a single sideband phase noise representation, the calculated RMS phase error and jitter results for our PLL converted to degrees and pS are as follows:

$$\theta_{rms} = 4.344° \qquad \sigma_{jrms} = 0.215\,pS$$

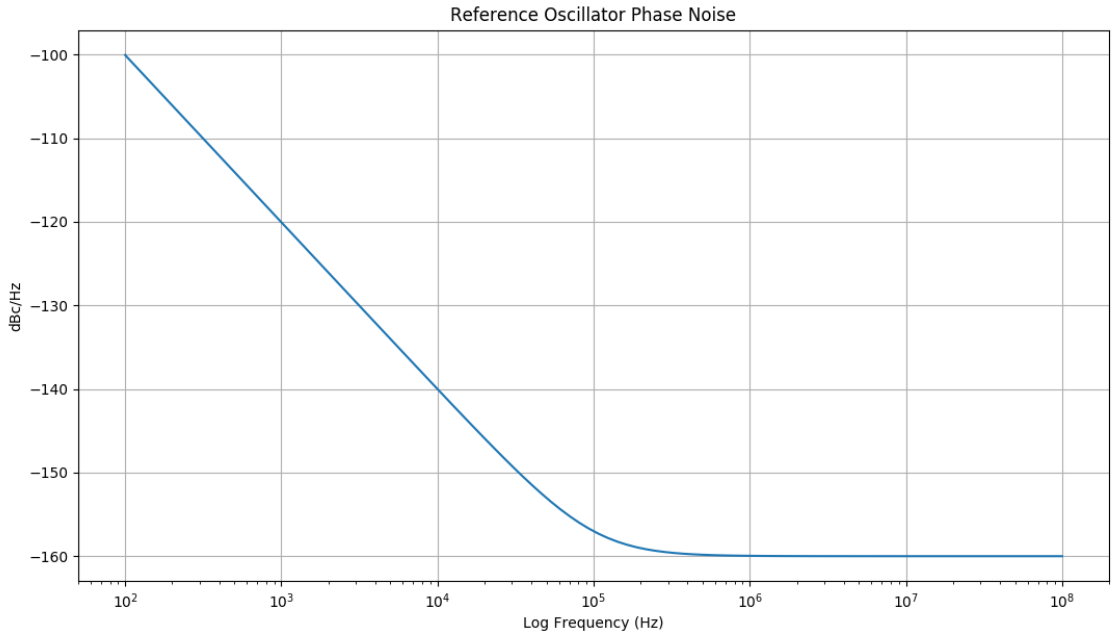

Figure 2: Reference Oscillator Phase Noise

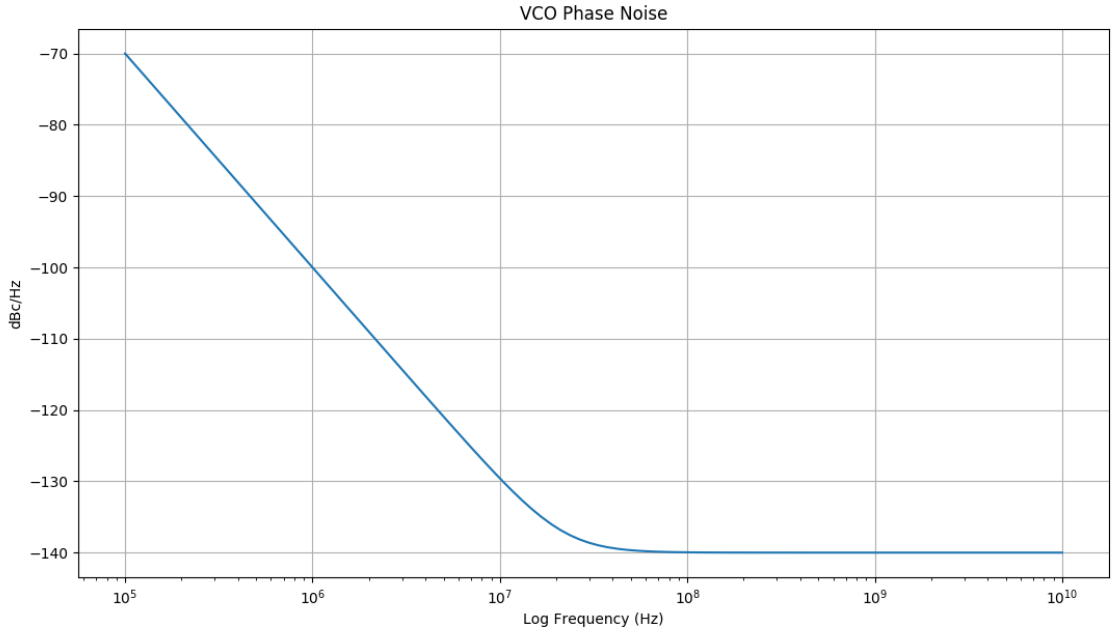

Figure 3: Voltage-controlled Oscillator Phase Noise

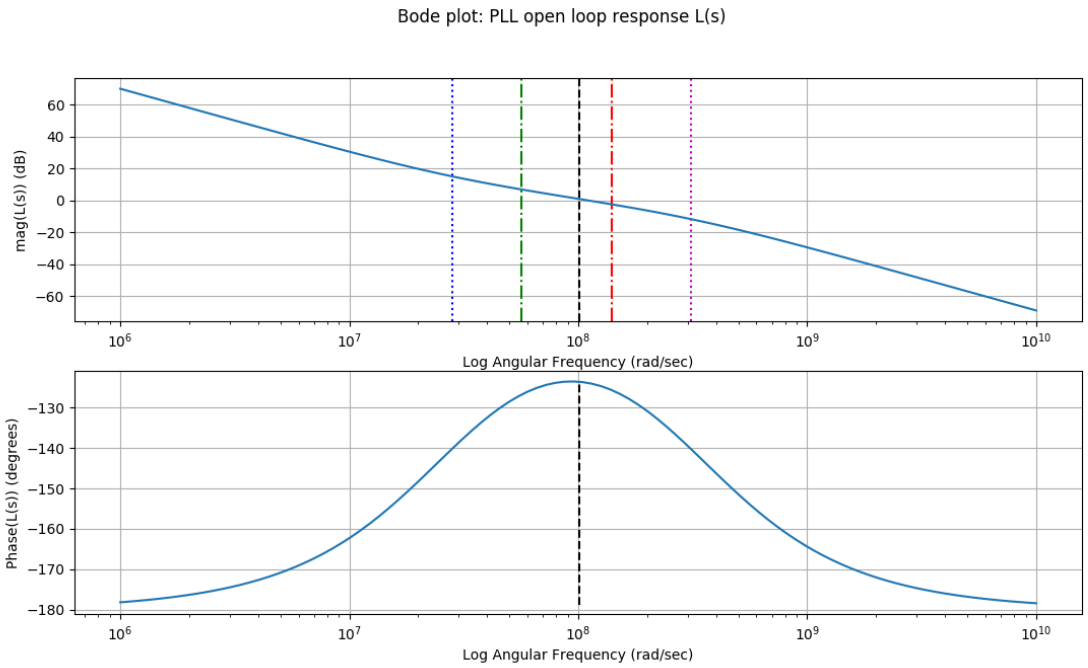

Figure 4b: PLL Open Loop Response

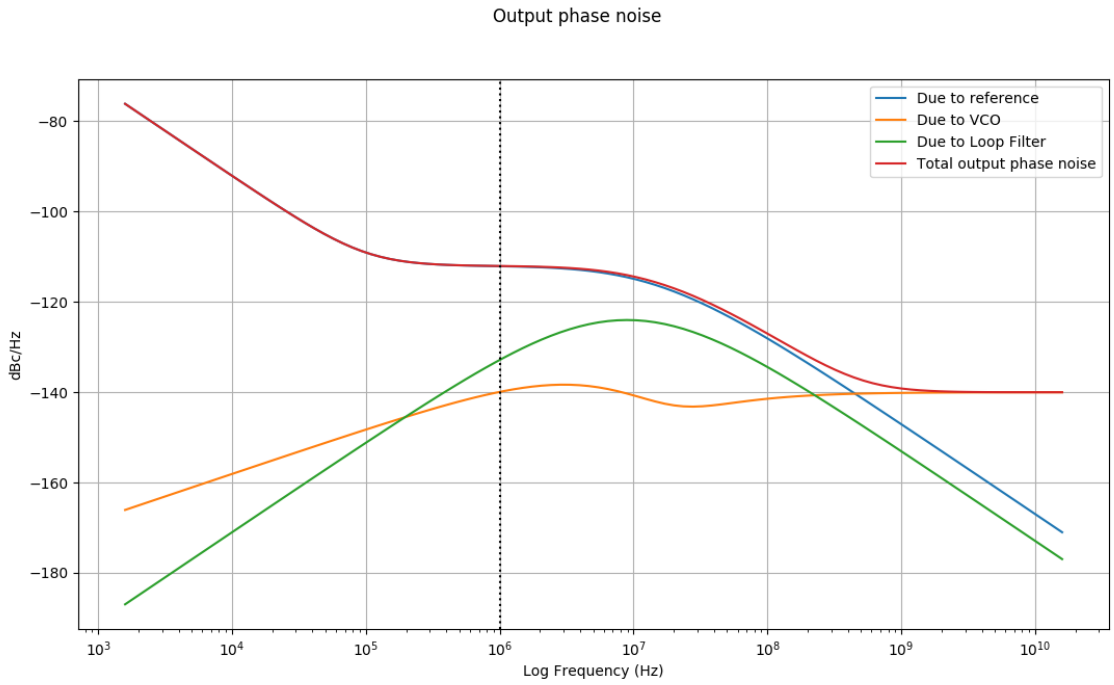

Figure 4d: PLL Output Phase Noise (with components)