Simulation and Design of CT Integrators and Filters

1. Opamp active-RC integrator simulation: The schematic entry for the active RC integrator was completed with the Verilog-A-modeled Opamp and the given parameter and supply/reference values. Subsequently a DC analysis was performed to calculate the DC operating point of the circuit.

a. Integrator small-signal response: To assess the small-signal response of the integrator, an AC Analysis was performed: the frequency was swept from 1KHz to 20GHz with an input AC signal of 1mV. (figure 2a displays the small-signal AC bode plot) From the simulation, the frequency response of the system was measured (low-pass):

$$H(w\to 0)=A_0=98.242\,v/v \quad \text{or} \quad 39.859\,dB$$
$$F_0=13.636\,MHz \quad \text{or} \quad w_0=85.678\,x10^6\,rads/sec$$
$$F_t=1.364\,GHz \quad \text{or} \quad w_t=8.568\,x10^9\,rads/sec$$

And to find the transfer function coefficients, recall:

$$H(s)=\frac{k_1 s+k_0}{s+w_0} \qquad H(0)=\frac{k_0}{w_0}\sim 100\,v/v \qquad H(w\to\infty)=0$$

Therefore:

$$w_0=85.678\,x10^6\,rads/s \quad , \quad k_0=8.568\,x10^9\,rads/s \quad , \quad k_1=0$$

b. Integrator transient response and linearity (Vin: 1mV): A transient simulation was performed for 20uS with an input signal of 1mV at 1MHz: the input and output signals' amplitude was plotted versus time (see figure 2b.1). In addition, a Fourier Transform (dft) was plotted to visualize the magnitude of the fundamental and harmonics distortion. (see figure 2b.2)

The magnitude difference in dB of the fundamental minus the largest harmonic was used to compute the SFDR (spurious free dynamic range) of the circuit response. The Cadence calculator was used to calculate the THD (total harmonic distortion), this figure was also confirmed by hand calculations.

$$SFDR=42.065\,dB \qquad THD=1.146\,\%$$

c. Integrator transient response and linearity (Vin: 0.1 V):

The previous transient simulation was repeated with a larger input signal of 1mV to assess the decrease in linearity of the circuit. The input and output signals were plotted in the time domain (see figure 2c.1) and the Fourier Transform was plotted to visualize the output signal in the frequency domain. (see figure 2c.2)

Lastly, the SFDR and THD FoM were calculated as before:

$$SFDR=10.991\,dB \qquad THD=37.71\,\%$$

d. MOSFET-C integrator frequency response

First, the original resistor in the circuit was replaced with an appropriately sized NMOSFET device operating in the triode region (pseudo-resistor). An AC analysis was then performed while sweeping the control voltage on the gate of the transistor to assess variation in the integrator frequency response. Finally the frequency response was plotted with a set control voltage of 0.7V. (figures 2d1 and 2d2 respectively)

2. Design: differential 2nd order band-pass GM-C filter:

With the following bandpass filter requirements:

Resonant Freq: $F_0=200\,MHz$ or $w_o=1.257\,x10^9\,rads/s$

Gain and quality (Q) factor: $H(w_0)=1\,v/v$, $Q=5$

And given capacitance values: $C_a=C_b=200\,fF$

First, Using the transfer function for a 2nd order filter (design form)

$$H(s)=\frac{k_2 s+k_1 s+k_0}{s^2+(w_0/Q)s+w_0^2} \quad \text{and band-pass coef.} \quad k_0=k_2=0$$

Then, computing $H(w_0)=1$ and solving for k_1 yields:

$$k_1=G(w_0/Q)=257.327\,x10^6\,rads/s$$

Finally, using the design equations for a biquad response:

$$C_x=C_b(k_2/(k_1-k_2))=0 \quad , \quad G_{m1}=w_o C_a=251.327\,\mu S$$
$$G_{m2}=w_0(C_b+C_x)=251.327\,\mu S \quad , \quad G_{m3}=G_{m2}/Q=50.265\,\mu S$$
$$G_{m4}=k_0 C_a/w_0=0 \qquad G_{m5}=k_1(C_b+C_x)=50.265\,\mu S$$

Having the required specs (note minor differences from slides), a fixed resistors transconductor topology was chosen, where:

$$I_o=\frac{V_{in}}{2/gm+R_s} \quad \text{and} \quad G_m=\frac{1}{2/gm+R_s}$$

and assuming $R_s\gg 1/gm$ it can be approximated initially:

$$I_o\approx V_{in}/R_s \quad \text{and} \quad G_m\approx 1/R_s$$

With this topology, in order to maximize the linearity of the circuit, the source resistances Rs should be increased while also increasing the transconductance (gm) of each of the transistors, this allows to preserve the gain (GM) of each stage and make it largely "independent" of the transistor's non-linearities. Furthermore, in order to maximize the gm for the NMOS devices and with a common-mode gate voltage of half-supply: the devices had to be operated in sub-threshold.

Design process: For reference, these are the general design steps followed for this transconductor topology and band-pass filter. (see figures 3a for the transconductor testbench and GM plots)

1. From GM, calculate approximate Rs and precise gm values.
2. Set initial parameters for first design iteration. (ideal passives)
3. Check operating region and gm of transistors. (sub-threshold)
4. Optimize cell parameters (width and bias current) to meet gm.
5. Compute and plot large GM for each transconductor stage.
6. Optimize source resistances to meet GM for each stage.
7. Test band-pass filter with designed transconductor cell.
8. Parametric optimization to meet exact filter requirements.
9. Optimize transconductors for linearity and power consumption.
10. Select IC resistor and size accordingly for desired resistance.
11. Select IC capacitor (MOMs are not available on library)
12. Test with non-ideal passives and a temperature of 65° Celsius.
13. Re-size resistors accordingly to meet performance at 65° C.
14. Assess filter performance under process variations.

Results: These are the simulated results for the filter at 65°

$F_0=208.93\,MHz$ $H(w_0)=1\,v/v=0\,dB$ $Q=5.732$

$*SFDR=11.99\,dB$ $P=1.1\,x(300\,\mu A+150\,\mu A)=495\,\mu W$

**for narrow bandpass filters a two tone distortion test should be used instead.*

Schematics: *See figures 3b for transconductor and biquad filter hierarchical drawings with annotated node voltages.*

Plots: *See figures 3c for small-signal frequency response, corner analyses, transient analyses and Fourier transform.*

Component values: $C_0=C_1=C_2=C_3=400\,fF$ (cfrm1)

For transconductors 3 and 5: $G_{m\,3,5}=56.01\,\mu S$ $I_{dc}=75\,\mu A$

$W=4\,\mu m$ $N_f=4$ $L=0.060\,\mu m$ $gm=996.9\,\mu S$

$r_w=0.24\,\mu m$ $r_l=17.1\,\mu m$ $R_s=13.270\,k\Omega$ (rnporpo)

For transconductors 1 and 2: $G_{m\,1,2}=301.31\,\mu S$

$I_{dc}=150\,\mu A$

$W=50\,\mu m$ $N_f=50$ $L=0.060\,\mu m$ $gm=2.742\,mS$

$r_w=0.24\,\mu m$ $r_l=2.75\,\mu m$ $R_s=2.063\,k\Omega$ (rnporpo)

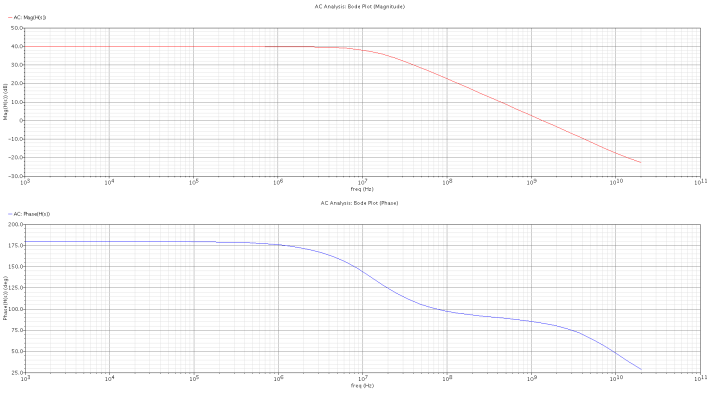

Figure 2a: Opamp Integrator Small-signal Response (Bode Plot)

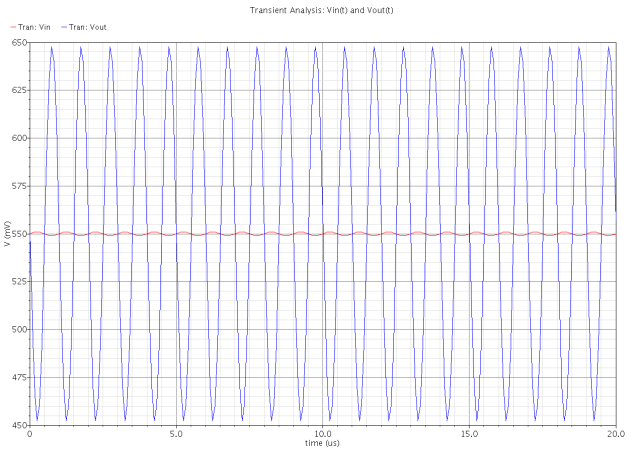

Figure 2b.1: Opamp Integrator Transient Response (Vin: 1mV)

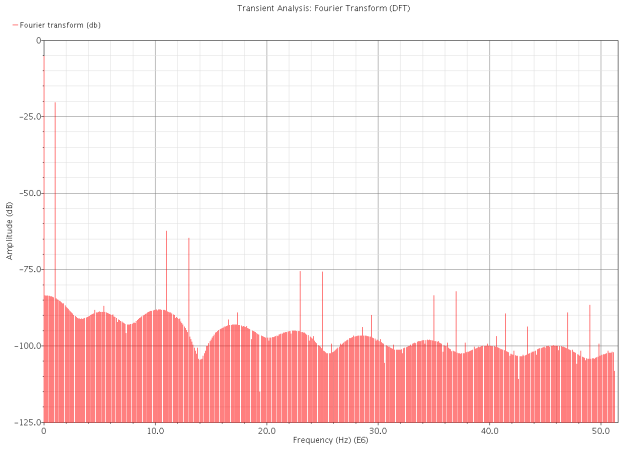

Figure 2b.2: Opamp Integrator Fourier Transform (Vin: 1mV)

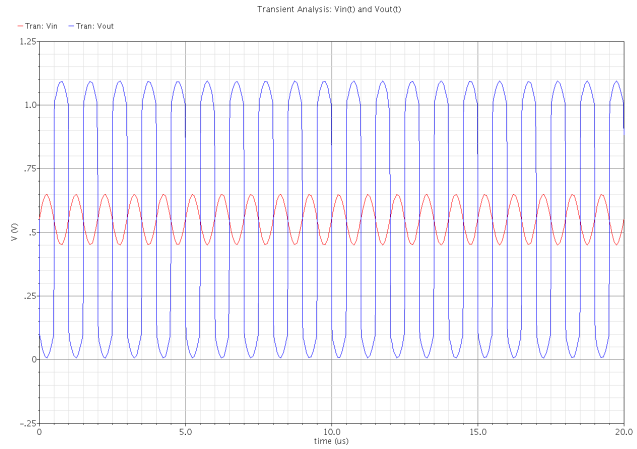

Figure 2c.1: Opamp Integrator Transient Response (Vin: 0.1V)

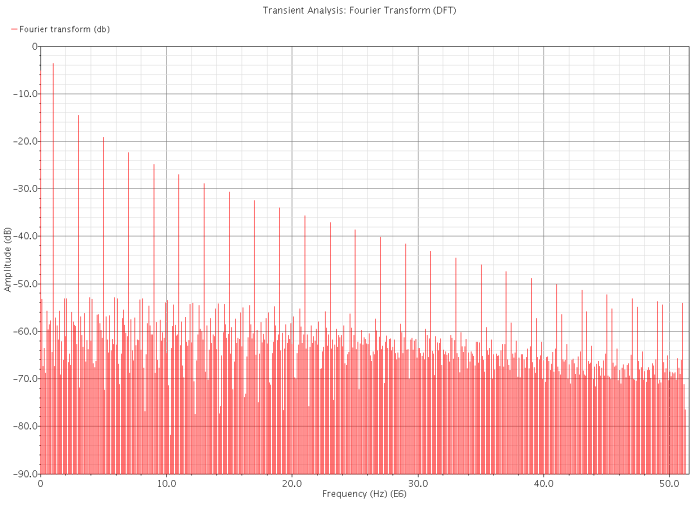

Figure 2c.2: Opamp Integrator Fourier Transform (Vin: 0.1V)

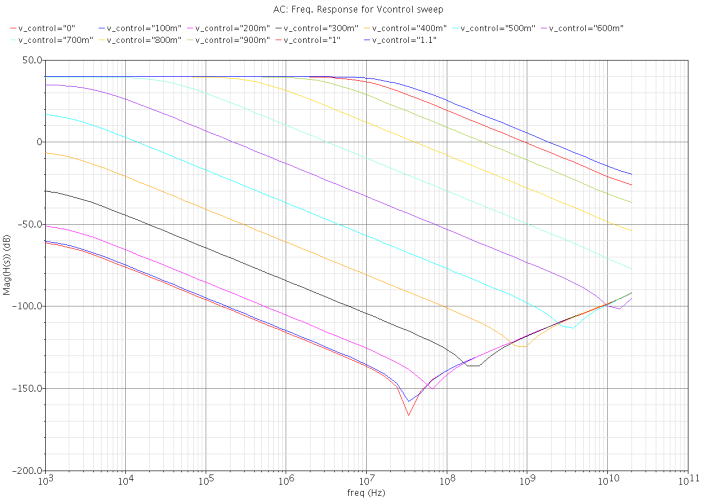

Figure 2d1: MOSFET-C integrator Response (Vcontrol sweep)

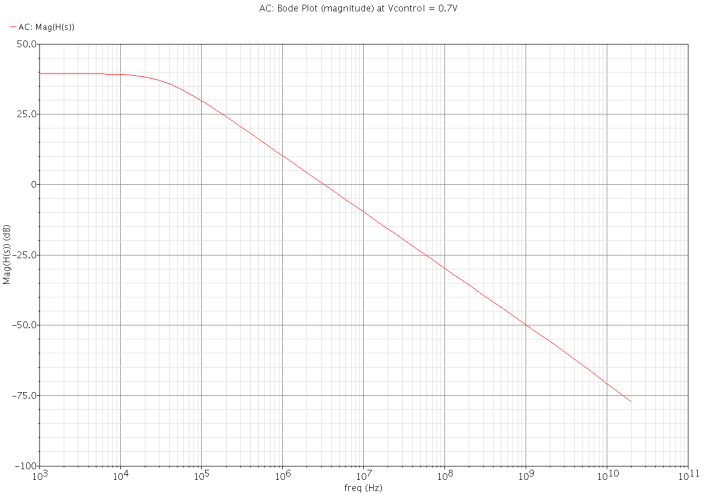

Figure 2d2: MOSFET-C integrator Response (Vcontrol: 0.7V)

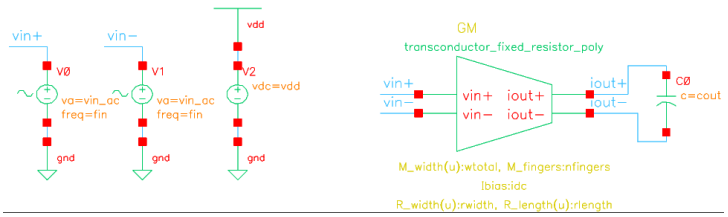

Figure 3a1: Parametric Transconductor Testbench
(see figures 3b1 and 3b2 below for transconductor cells)

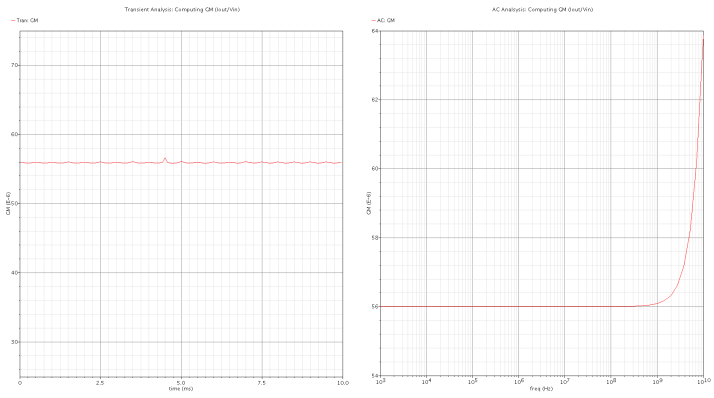

Figure 3a2: Measured GM Values from Transconductor Testbench

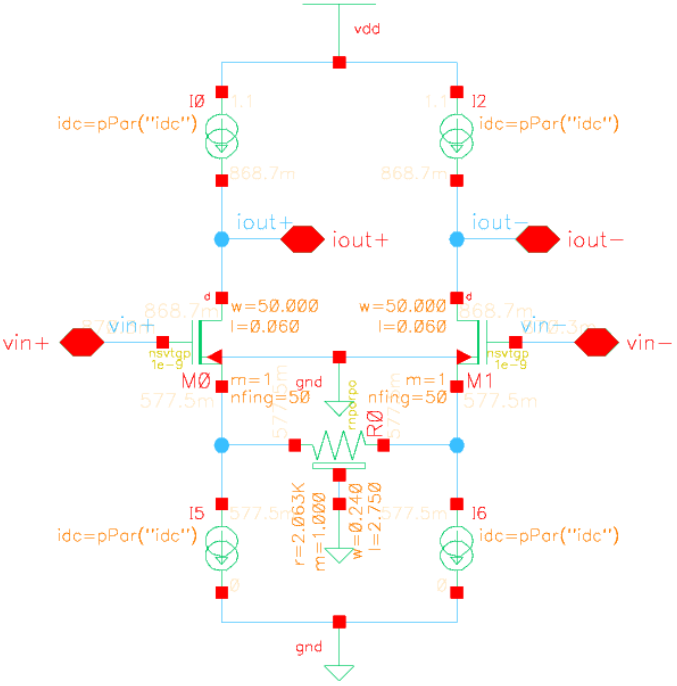

Figure 3b1: Transconductor cell (GM1 and 2) with Node Voltages

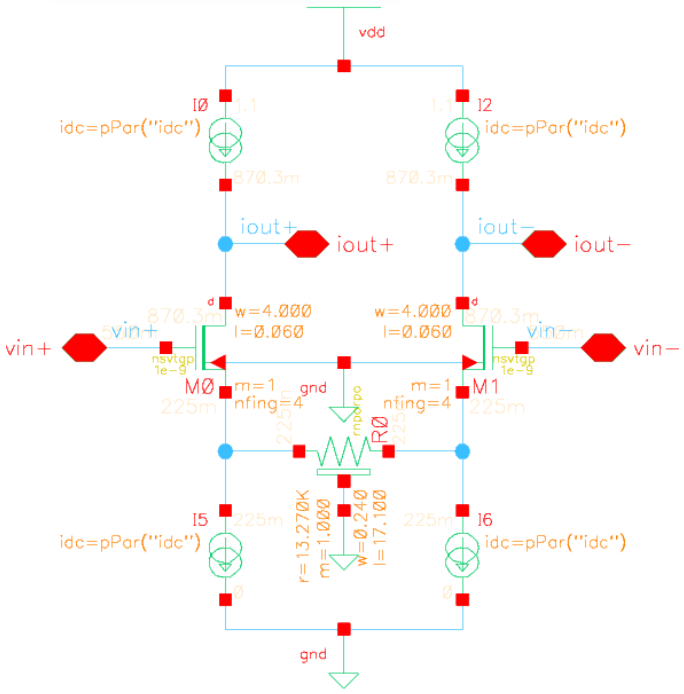

Figure 3b2: Transconductor cell (GM3 and 5) with Node Voltages

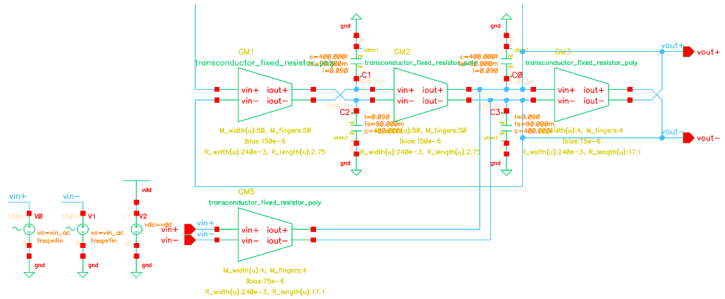

Figure 3b3: Differential 2nd Order Band-pass GM-C filter

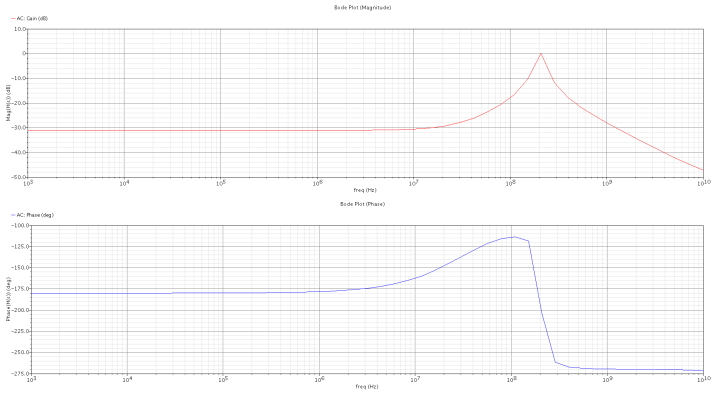

Figure 3c1: Band-pass Filter Frequency Response (bode plot)

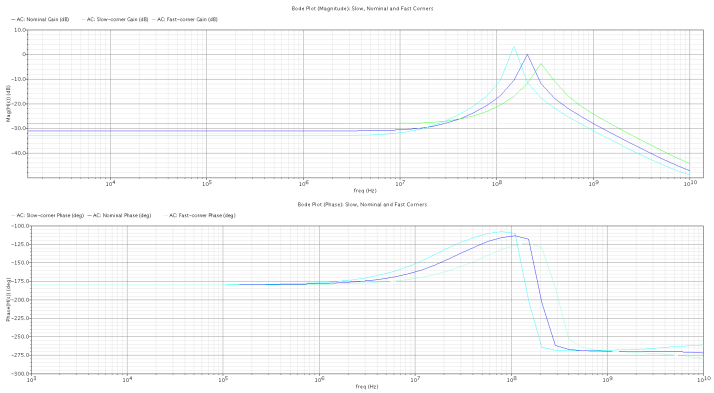

Figure 3c2: Band-pass Filter at Slow, Nominal and Fast Corners

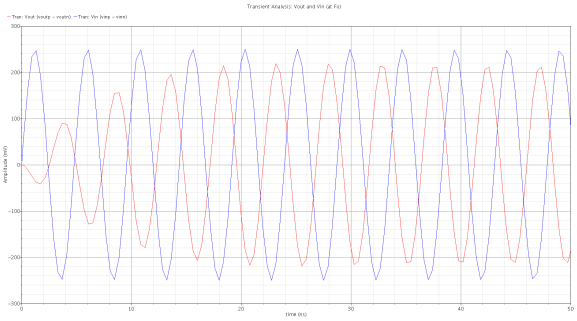

Figure 3c3: Band-pass GM-C Filter Transient Response (at Fo)

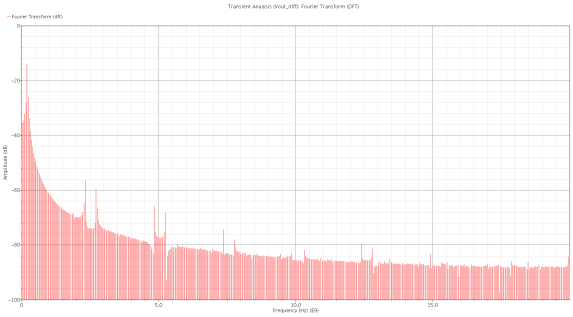

Figure 3c4: Band-pass GM-C Filter Fourier Transform (at Fo)