PVT Invariant Voltage Controlled Low Pass Filter

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Abstract— **The scope of this lab was to cultivate on the low pass filter implemented in lab two by designing a filter tuning algorithm which automatically tunes to a user's desired filter corner frequency Fc. The tuning band is predefined from 15KHz to 30KHz with a maximum step size of 0.7KHz. To successfully complete this project we had to interface analog and digital techniques to meet the design specs. This project is important and very practical since it can be applied in cell phone technology to improve signal quality as it removes unwanted interferences and provide reliability to account for changing temperature conditions. An excellent application of this design project in our opinions is in the following scenario: In today's competitive economy new mobile devices are being developed every day and one of the fundamental requirements is reliability. A mobile device that is immune to weather conditions and that will self-calibrate as needed is a huge asset as it can be marketed to be sold anywhere in the world not just where it was produced.**

PVT Invariance; Self Calibration; Mixed Signal Filter; Low pass filter

I. INTRODUCTION

This lab was an excellent method of encouraging students to apply the various Op-Amp circuit topologies learned in lecture to realizing an actual physical system that performs a pretty sophisticated algorithm. Besides the 12th order Butterworth filter produced in lab two, our calibration had many different analog components including a peak detector which implemented forward and reverse biased diodes connected to capacitors to capture both the positive and negative peaks of a sine wave and a difference amplifier to calculate the peak to peak amplitude. A voltage controlled oscillator was accomplished with an Integrator followed by a Schmidt Trigger in the form of a comparator. Buffers to eliminate loading were used to transfer the total voltage from the output of one system to the input of another. Summing amplifiers were also used for interfacing digital and analog signals. A voltage regulator of 5V was used to power the various digital modules including the microcontroller, the D/A converter and the switches. Some extra features were also used to improve the user interface. A normally open switch to reset the microcontroller and two LEDs were used to indicate the state of calibration; one LED indicated calibration in process while the other LED specified the conclusion of the calibration routine.

II. BODY

A. Design Considerations

For this design the major constraint was time, these constraint was the main determinant for the use of an integrated digital/analog approach as the team had a decent knowledge of embedded systems, a complete analog approach however would have involved more extensive research and would have made it harder for us to meet the deadlines. After an embedded path was chosen several different approaches were considered. The first approach was similar to that discussed in class, by making the poles of our filter sit right on the jw axis it would have been possible for us to turn the low pass filter into an oscillator with the oscillation frequency proportional to the cutoff frequency of the filter, then measuring the frequency via the microcontroller would have been a trivial task via the use of a timer interrupt and a counting routine, after that, all that would have been left would be the modulation of the common control voltage for the whole low pass filter, these modulation after several iterations would have allowed us to converge into the desired cutoff frequency. This approach however simple for other filter topologies proved to be quite complex for our chosen topology due to the fact that we did not have direct control of the distance of the poles from the jw axis, in other words the peaking for each stage was given by a ratio of capacitors which were very sensitive to component tolerances. Another option considering the fact that we were using a Butterworth approximation would have been to calibrate a second order dummy stage and then apply the same control voltage to the whole low pass filter, while this would have worked for an ideal Butterworth Low pass filter where all the stages are tuned to the same cutoff frequency our gm-C filter required slight tuning for each stage due to the fact that the Q values were not exactly Ideal, therefore after multiple thought experiments the team decided to follow a different path.

The second potential design that was considered was a simplified version of the final chosen design. From the previous thought experiments we concluded that design ideas that involved the movement of the poles parallel to the real axis would impose severe hurdles in the implementation stage of our algorithm, further the team concluded that manipulating the working low pass filter would impose high risks due to the high order of the low pass filter and the high sensitivity of the

filter's response to single component tolerances. For this reason we decided to pursue designs that exploited tuning the cutoff frequency as this was very easily accomplished with our circuit, further the use of this approach would imply that we could treat our filter as a single integrated block with two inputs (input signal, control voltage) and one output (filtered response).

We realized that we could use the microcontroller to mimic the series of steps that we performed when manually tuning the filter to a desired cutoff frequency. For this to be possible the microcontroller would have to have access to a voltage controlled oscillator (analogous to the function generator) a peak to peak detector (analogous to the oscilloscope peak to peak measure), some digital/analog interfacing and an analog signal switching mechanism.

The initial algorithm was visualized to follow the steps needed to calibrate the filter manually in the following way: Initially a low frequency sine wave was introduced into the low pass filter, the peak to peak amplitude was measured at the output of the filter and the -3db peak to peak voltage calculated, after that a sine wave with the desired cutoff frequency was introduced into the circuit and the control voltage to the whole low pass filter was modulated until the measured peak to peak amplitude was equal to the -3db peak to peak voltage calculated previously, at this point the circuit was calibrated to the desired cutoff frequency.

The first potential big hurdle encountered with this design was the generation of a voltage controlled sine wave. Most of the information found during our research implied that achieving a sine wave oscillator with a fixed frequency would have been attainable both via the analog domain or the digital domain, a voltage controlled sine wave oscillator however seemed a more complex issue with integrated chips in monolithic form dedicated solely to synthetizing variable frequency sine waves. After more thought was put into this and after aiming to understand the internal structure of sine wave generators from their datasheets the team realized that most of them made use of a triangular wave generator and sine wave shapers. Pursuing the reason for the common use of triangular wave generators the team arrived at the needed answer, triangular waves present harmonics only at odd multiples of the main frequency with the magnitude of this harmonics much lower than that found for square waves. Taking this reasoning even further the team realized that due to the high order of our low pass filter, keeping the base frequency high enough so as to keep the harmonics in the stop band will virtually make the triangular wave look just like a sine wave and the fact that we were using a Butterworth maximally flat approximation would allow us to measure the dc gain response of the filter at higher frequencies so as to allow us to keep the harmonics always in the stop band. The conclusion of this reasoning was therefore that instead of using a pure sine wave voltage controlled oscillator we could use a triangular wave VCO with decreased complexity.

Another important milestone that needed some thought was the implementation of the peak to peak detector, ideally this device would calculate the positive peak, the negative peak and then take the difference between them, several design choices were considered with the last two candidates being the common diode capacitor peak detector and the diode capacitor Op Amp peak detector (to eliminate diode drop). The finalist was the common diode capacitor peak detector due to the fact that under the negative peak the Op Amp in the positive peak detector will be operating open loop which introduced some instability to the response. The difference of the peak detectors was visualized for implementation simply via the use of a difference amplifier. However desirable and simplistic, this design approach had a potential flaw and it was the error introduced by the diode drop in both the positive and the negative peak detector which would lead the low pass filter to converge towards an erroneous cutoff frequency, the team decided that due to the small nature of the error, a linear approximation of the error would diminish the error significantly and keep it within bounds.

Two important building blocks left to discuss are the realization of the digital/analog interface and the switching between calibration mode and input mode for our circuit. Due to the familiarity of the team with the use of both digital to analog converters and analog to digital converters the only interfacing required was scaling and offsetting the analog signals to make sure that they all remained between 0 to 5V maximum and amplifying and offsetting DAC signals to provide for needed negative voltages or voltages higher than 5V, this was visualized as a simple implementation of either difference amplifiers or summing amplifiers with gain. The switching between input and calibration mode was thought at first to be an easy design via the use of both N-channel Mosfets and P-channel Mosfets however after further research it was discovered that such an approach will lead to massive distortion, for this reason the team decided to look into an integrated chip that would perform this switching task and found several quad packages available for switching analog and digital signals.

B. Impelmentation & Design

The design decisions indicated previously led us to the finalized block diagram referenced in Appendix B.1 with a control scheme described by the state diagram in Appendix B.2, the aim in this section will be to explain the calibration algorithm via a small thought experiment (The reader is advised to follow the thought experiment using the illustrated block diagram) and then expand more deeply into the individual blocks in the system diagram. The thought experiment will start by the application of a desired Set Point voltage transformed into frequency by equation 1. The analog to digital converter inputs this value into the microcontroller which instructs the analog switch to switch to calibration mode and inhibit any input signal, following this action the microcontroller gets ready to input a low frequency signal to the low pass filter and it does so via the VCO. First it sends an arbitrary control voltage via the digital to analog converter to the voltage controlled oscillator, the microcontroller then reads the frequency output of the VCO and performing a real time binary search algorithm

converges into the value of 11 KHz (low frequency signal used to measure the dc response of filter). At this point the microcontroller makes use of the analog peak to peak detector to measure the dc gain of the filter; it uses this value to calculate the -3db peak to peak voltage. Now the microcontroller restarts the VCO by sending it an arbitrary voltage, it then reads the output frequency of the VCO and modulates the input voltage of the VCO until the output frequency converges to the cutoff frequency desired by the user. Having done that the microcontroller reads the peak to peak voltage from the peak detector and starts to modulate the control voltage input to the adjustable low pass filter until the peak to peak voltage matches the previously calculated -3db peak to peak voltage, at that point the gm-C filter is successfully calibrated and the microcontroller instructs the analog switch to allow the input signal into the low pass filter and starts monitoring changes in the desired cutoff frequency to assess if it needs to recalibrate the system.

The following are the equations used to calculate the desired frequency from the voltage Set Point (simply a line equation relating 0 – 5V to 15 – 30 KHz)

Desired Cutoff Frequency:

$$F_c = 3000 * V_{in} + 15000 \quad Hz \quad\quad (1)$$

Desired Voltage Set Point:

$$V_{in} = 0.000333 * F_c - 5 \quad V \quad\quad (2)$$

The control module (Microcontroller) in the system was implemented using an Atmega 328P with an arduino ISP, the microcontroller had 10 bit integrated analog to digital converters and was clocked with an external 16MHz crystal oscillator for added timing accuracy. The frequency measurement from the VCO was accomplished via the use of a timer interrupt that gave us a measuring window of 15 ms, in this window the microcontroller counted the transitions from low to high and high to low and after the time was up it used the following formula to calculated the frequency of the input signal.

Microcontroller Frequency Calculation

$$VCO_{freq} = \frac{(\# \ of \ ticks)/2}{(time \ window)}$$

The digital to analog converters (LTC 1661) were two 10 bit integrated serial DAC's in a single monolithic Integrated IC, the DAC serial timing scheme was programmed into the microcontroller. The analog switch block of the circuit was implemented via the use of a quad analog/digital switch (CD 4016). The serial communication scheme (9600 baud rate) was established to provide debugging capabilities to our system.

The Triangular/Square voltage controller oscillator was constructed via the use of an integrator and an inverting Schmitt Trigger (comparator LM339) connected in a feedback loop. At the output of the Schmitt Trigger an N-Channel Mosfet was used to discharge the integrator capacitor periodically. The Triangular and Square wave outputs of the VCO were gathered from the output of the integrator and the Schmitt Trigger respectively.

The peak to peak voltage detector was a composite circuit involving the use of a positive peak detector (forward diode and capacitor) a negative peak detector (reverse biased diode and capacitor) and a difference amplifier which evolved into a simplified instrumentation amplifier to provide high input impedance and reduce loading effects at the input. The general purpose quad operational amplifiers used to provide the digital to analog interface were the following: MC3403, LM348N and HA3-4741.

The filter configuration was identical to that used for the previous project with the idealized second order building block (Appendix C.1) , the final implementation of the second order building block (Appendix C.2), the circuit schematic displaying the complete 12th Order gm-C Butterworth Voltage Controlled Low Pass filter (Appendix C.3) and the equations used to describe the circuits remaining unchanged.

III. RESULTS

A detailed table with the project key results is displayed in Appendix A.2, Some important results include the power supply rails which the team decided to keep unchanged from lab 2 at +/- 12 V, the total power consumption of the circuit which increased to 734.4 mW due to the added digital and analog circuitry, the attenuation figures which remained both at the same values recorded from lab 2 at both 15KHz and 30 KHz, the pass band ripple which increased by 0.2 dB from the previous lab, the maximum frequency step size which now assumed a discrete value due to the 10 bit resolution of the Analog to digital converter and the average calibration error which is defined as the deviation from the user desired cutoff frequency which was measured to be +/- 200 Hz and which will be discussed in great detail in the following section. A table with a detailed description of the number and type of components used and the total cost was put together in appendix A.1.

IV. DISCUSSION

As was presented in the previous section a figure that deserves discussion is the considerable average calibration error. In spite of the fact that the error is within bounds the team decided to embark in some intuitive research to try to discover the nature of this error. After multiple hypothesis and discussion of ideas the team came into the conclusion that the error was due to the nature of the response of the peak detector at low frequencies. The peak to peak detector was visualized to provide a clean DC reading to the microcontroller for further processing irrelevant of the output signal coming from the gm-C Filter, however as the frequency decreased the output of the peak detector starting introducing some noise into the signal. As it turns out this has to do with the capacitance value chosen for the peak detector, low capacitance capacitor values don't require a lot of charge to be fully charged and thus can oscillate and follow the input signal, given an approximate diode drop of 0.65 volts the capacitors voltage at the upper plate of a small capacitor will oscillate 0.65 volts from the peak until the diode becomes reverse biased so instead of getting a dc level at the upper plate of the capacitor indicating a peak voltage you get a value changing from the peak level to ~0.65 volts below that which makes the peak voltage reading quite inaccurate. There are two ways that we visualized to solve this small issue, the first way was by increasing the capacitance which will bypass the high frequencies to ground and we will end up getting a clean DC at its upper plate, this will however sacrifice the response speed of the peak detector to real changes in peak amplitude of the output waveform and the second way around this issue was to take the average of a big number of samples from the peak detector in the microcontroller thus virtually low pass filtering the signal, when asked about something that the team will have done different for the completion of this project this is the one factor that we would have looked more into, otherwise the team is pleased with the outcome of this project.

V. CONCLUSION

Although meeting the required deadlines for this project was challenging, this project was a great realization and physical application of the concepts learned in lecture in the domain of analog circuit design with the support of some digital technology.   Having insight into basic Op-Amp circuit topologies such as inverting/non-inverting amplifiers, summing/difference amplifiers, buffers, Integrators and Differentiators, which are the basic building blocks of our tuning algorithm, greatly benefited us especially when the circuit didn't behave as expected and necessary troubleshooting had to be performed.   One of the biggest challenges encountered in this project was getting the individual systems to replicate the performance obtained when tested individually.

While some components could have been implemented as ICs such as the voltage controlled oscillator, we preferred to build as much of the tuning algorithm as possible from discrete passive/active components. A lot of things were learned about the behavior of a physical system as compared to the ideal behavior experienced during simulation, an example of this was the VCO we implemented. The oscillator worked perfectly at times and then suddenly would completely stop oscillating. We theorized that since in order to achieve oscillation we had to ensure that the poles were on the jw axis, as soon as the poles shifted either to the right or to the left of the jw axis the system will stop oscillating. The problem turned out to be simpler than that involving a burned Mosfet and a faulty wiring issue. With a lot of hard work and dedication we were able to successfully complete the project requirements on time and build an efficient tuning algorithm to automatically modulate a 12th order low pass Butterworth's filter corner frequency from 15KHz to 30KHz.

REFERENCES

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A. Performance Specifications

A.1 Cost Analysis

Component	Quantity	Cost Per Unit	Total Cost
LM13700	6	1.98	11.88
Electrolitic Capacitors Misc	9	0.01	0.09
Ceramic Capacitors Misc	14	0.01	0.14
Resistors 1% Tolerance	102	0.01	1.02
Potentiometers	4	0.1	0.4
MC3403	2	0.51	1.02
LM348	2	0.54	1.08
HA3-4741	1	0.70	0.70
LM339	1	0.36	0.36
CD4016	1	0.44	0.44
LTC1661	1	3.39	3.39
Diodes (1N4148)	8	0.20	0.216
16 MHz Crystal Oscillator	1	2.30	2.30
LED's	2	0.20	0.40
7805 (5V Linear Regulator)	1	0.49	0.49
ATMEGA 328p uController	1	3.160	3.160
Push Button Switch	1	0.30	0.30
Total			27.386

Table 1: Cost Analysis

Parameter	Design Specifications	Results
Power Supply	Supply Rails	+/- 12V
Power Consumption	Current Consumption (+12V)	40.3 mA
	Current Consumption (-12V)	20.9 mA
	Power Consumption (+ 12V)	483.6 mW
	Power Consumption (-12V)	250.8 mW
	Total Power Consumption	734.4 mW
Functionality	Attenuation at 2fc (15KHz)	63 dB
	Attenuation at 2fc (30KHz)	62 dB
	Pass band Ripple (15KHz)	2.1 dB
	Pass band Ripple (30 KHz)	1.9dB
	Tunable from 15KHz – 30KHz	Yes
	Maximum Frequency Step Size (Given by 10 bit resolution of ADC)	15 Hz
	Average Calibration Error*	+/- 200 Hz
Cost Measure	Cost of Components	27.40 USD
Extra Parameters	Use of External Reference Oscillator	No

Table 2: Key Specifications Table

* This figure and the reason for the error is discussed in the discussion section

A.3 *Labview Frequency Sweep Response (Cutoff Frequencies: Fc: 15KHz, 22.5KHz, 30KHz)*
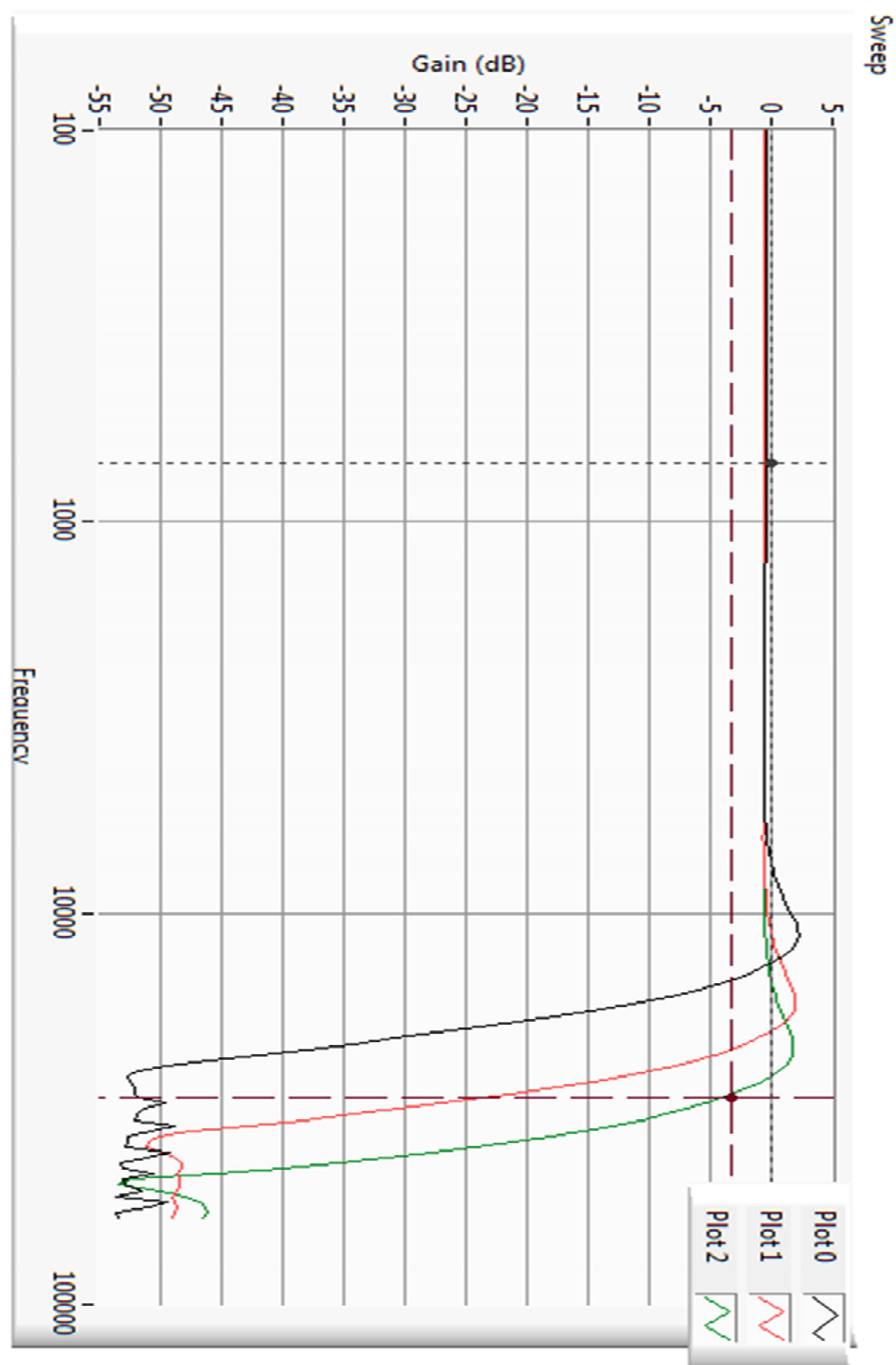
Figure 1: LabView Frequency Sweep Response (Fc: 15KHz, 22.5 KHz & 30KHz)

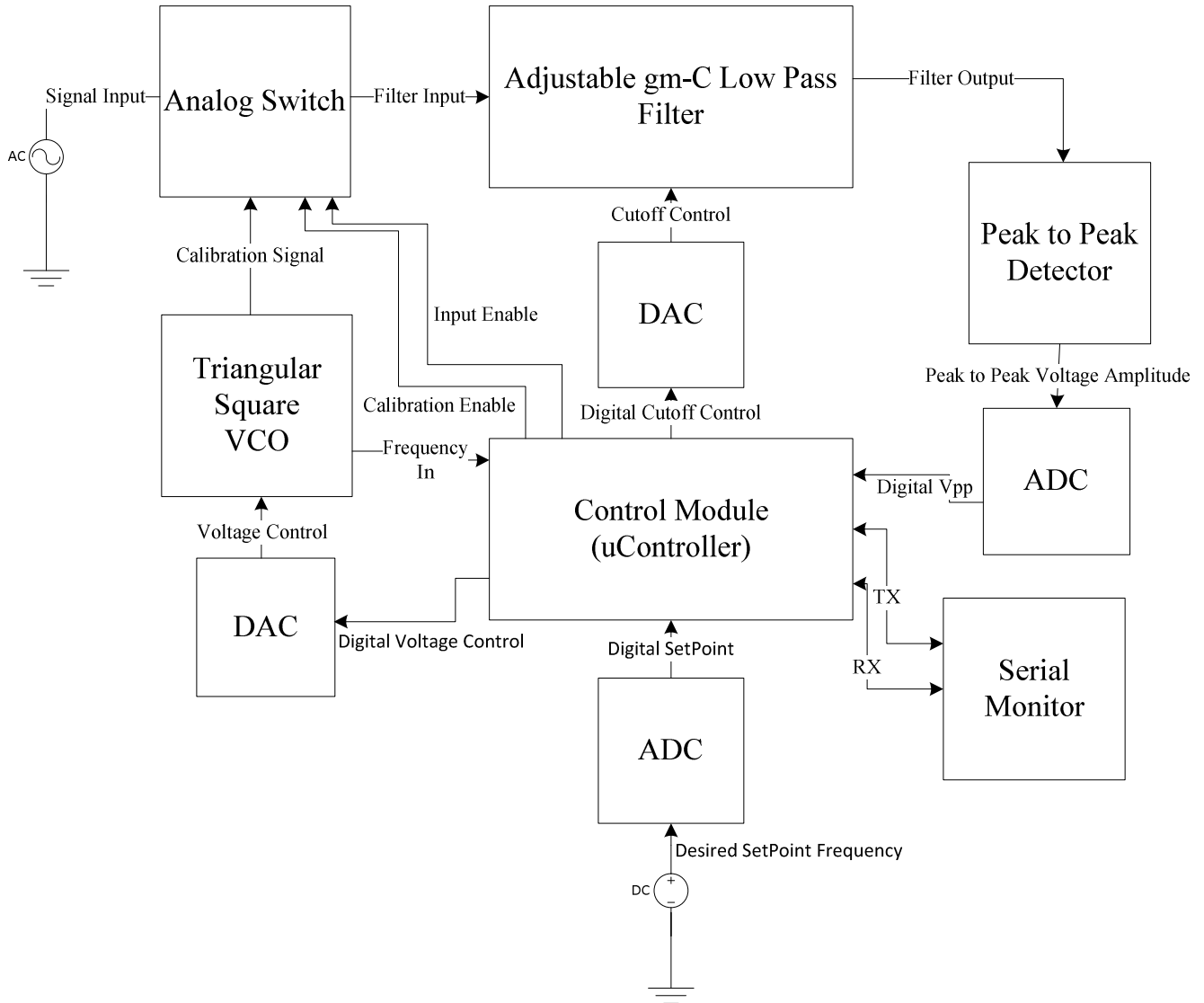*B. Design Diagrams*

B.1 Calibration Circuit Block Diagram

Figure 2: Calibration Circuit Block Diagram

PWR

A

B

E — F < 11 KHz — C — F > 11 KHz — D

F = 11 KHz

F

G

J ← F < Fdesired — H — F < Fdesired → I

F = Fdesired

M ← Vpp < V(-3db) — K — Vpp > V(-3db) → L

Vpp = V(-3dB)

N

newSetPoint != oldSetPoint

O

oldSetPoint = newSetPoint

Figure 3: Calibration Algorithm State Diagram

C. Circuit Schematics

C.1 gm-C Second Order Ideal Low Pass Filter Building Blocks
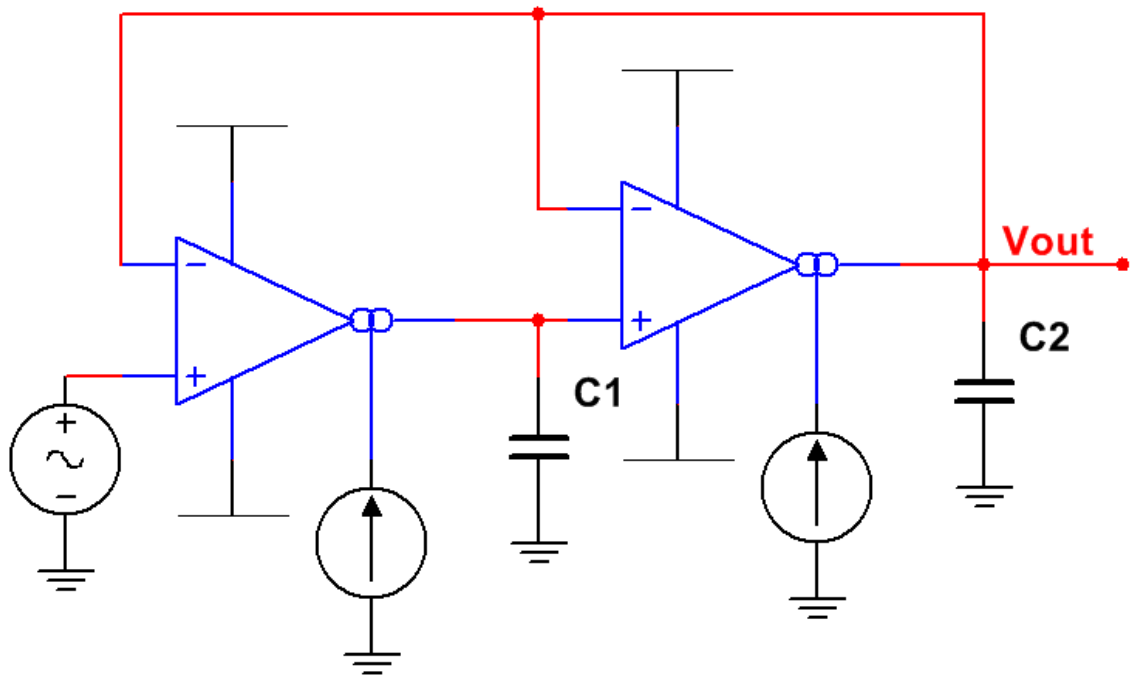
Figure 4: Idealized Second Order Low Pass Building Block

C.2 gm-C Second Order Low Pass Filter Realized Building Blocks
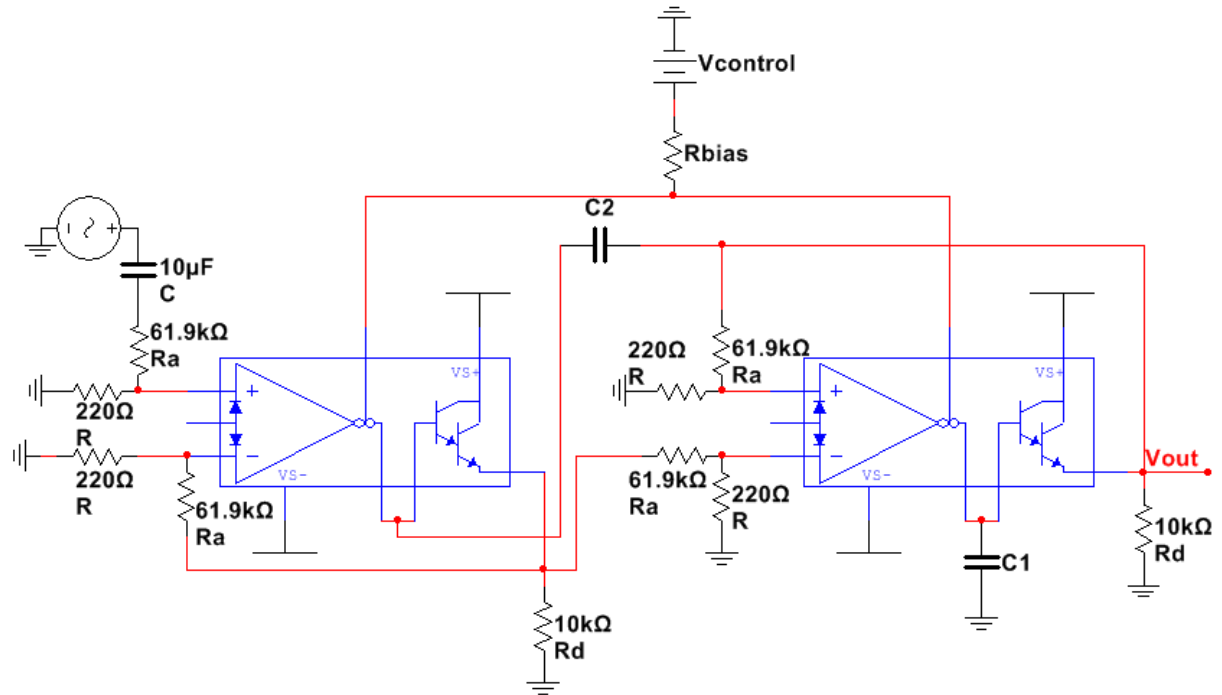
Figure 5: Final Implementation of Second Order Low Pass Building Block

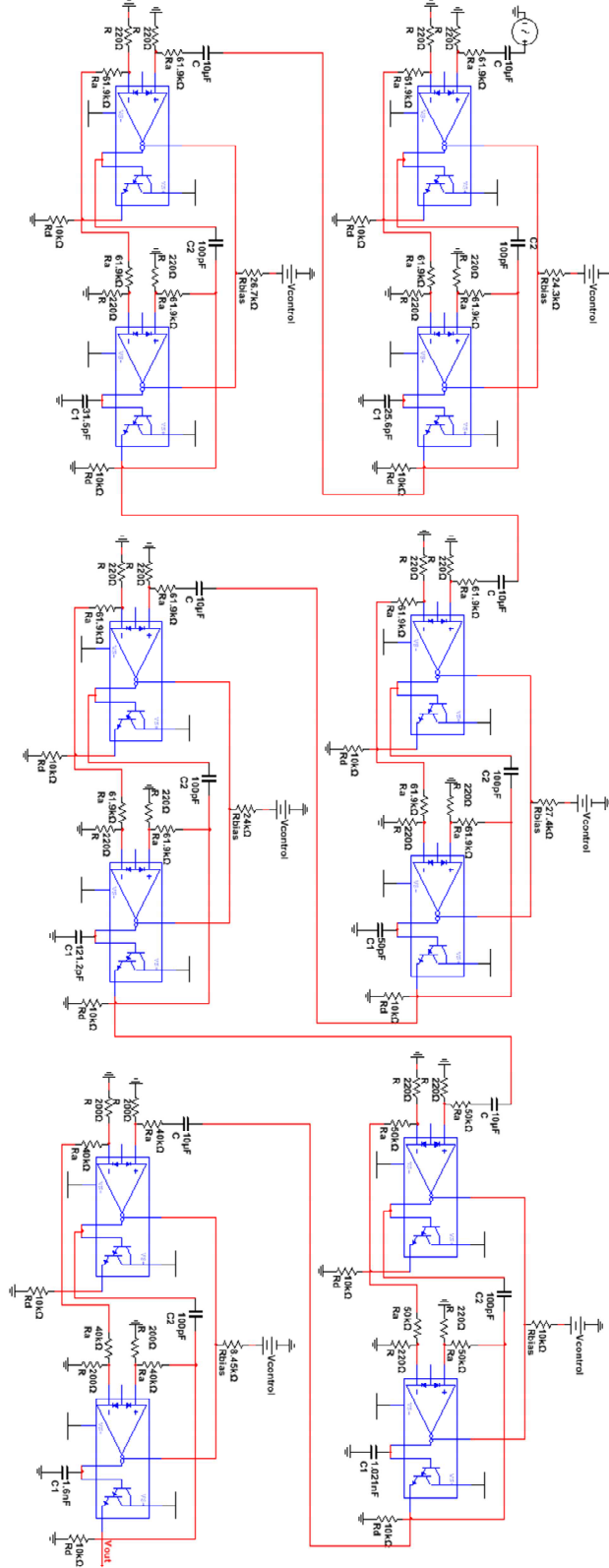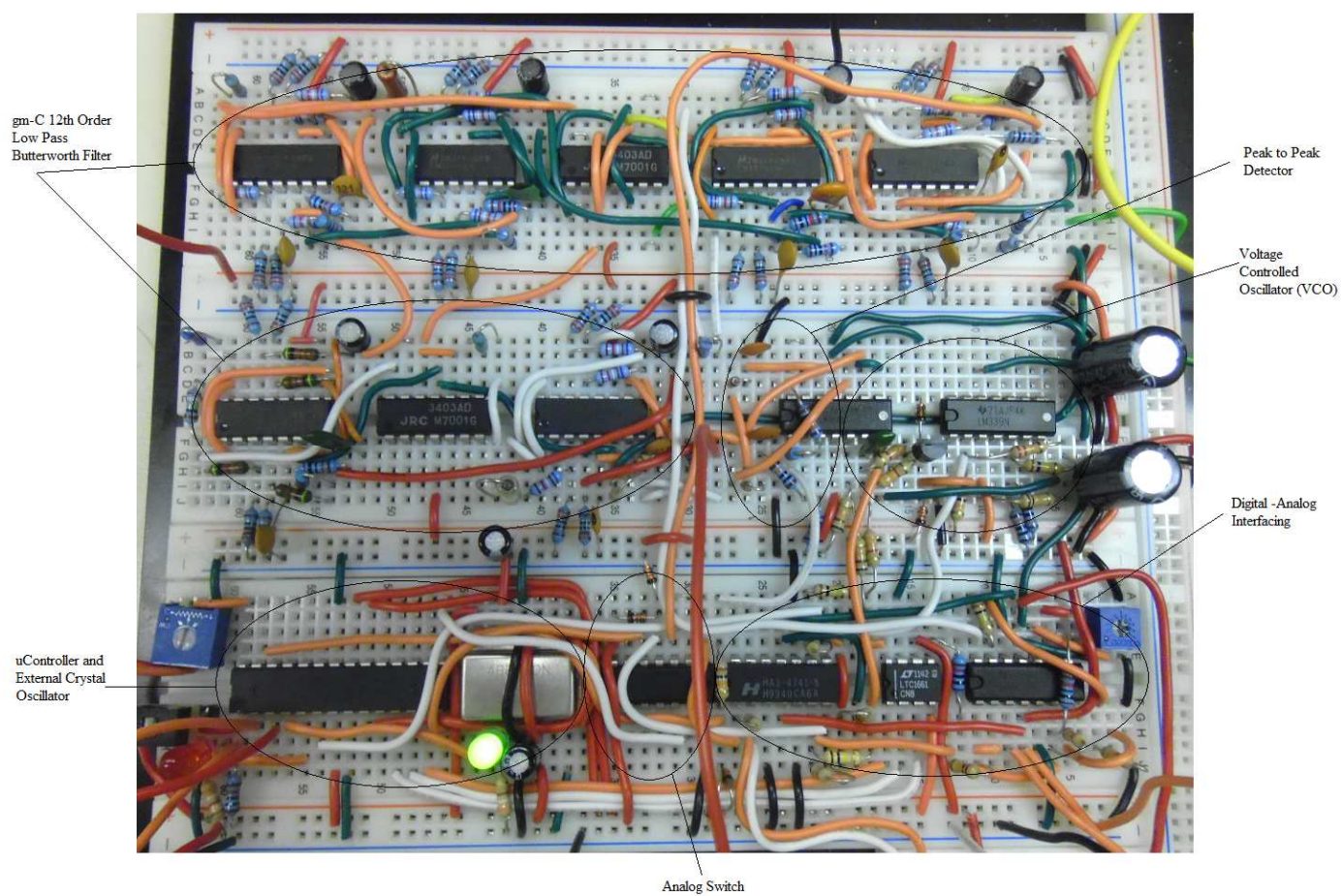Figure 6: 12th Order Tunable Butterworth Low Pass Filter Schematic

Figure 7: Photograph of Complete PVT Invariant Tunable gm-C Filter